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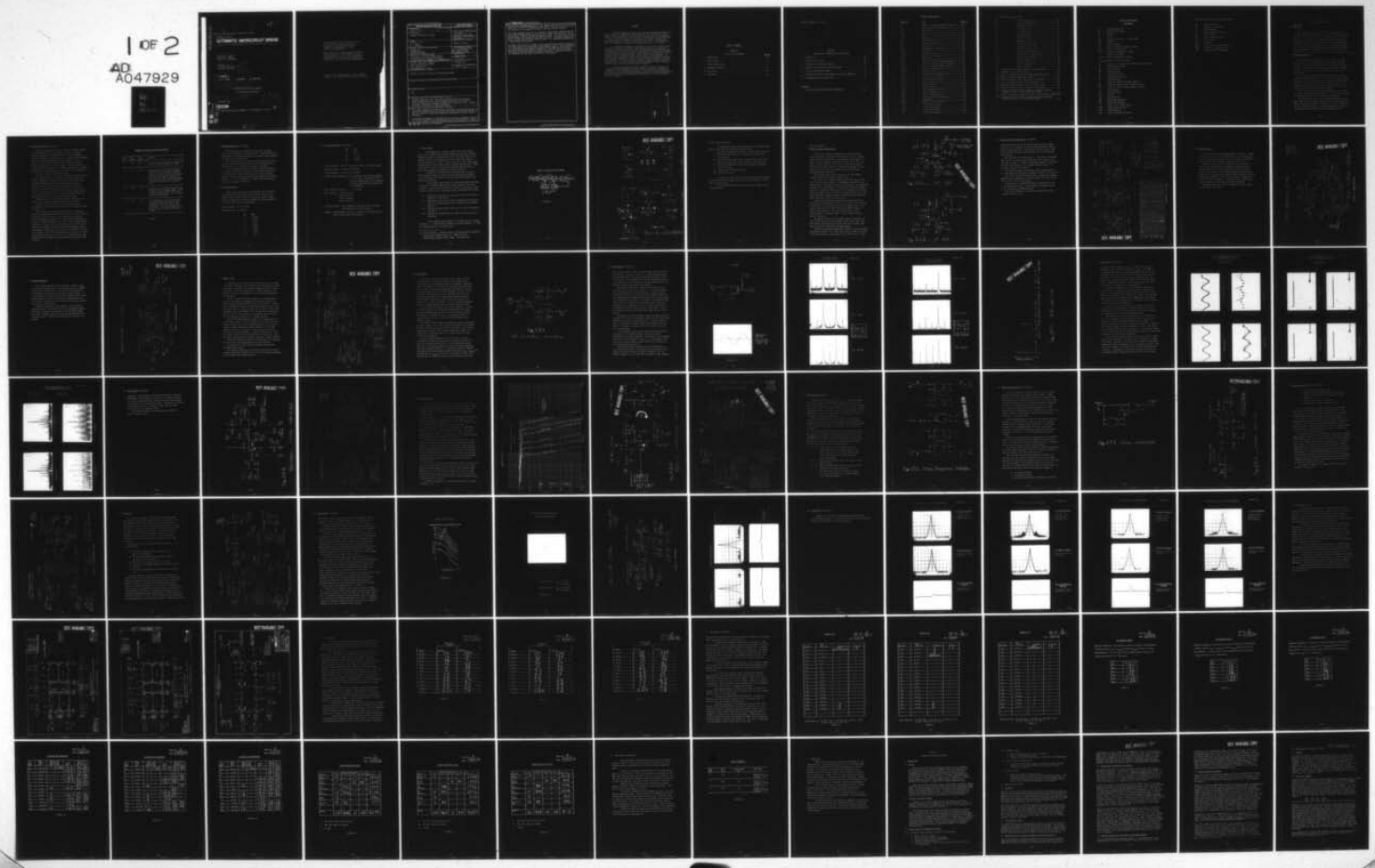

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Research and Development Technical Report

ECOM-75-1341-F

AUTOMATIC MICROCIRCUIT BRIDGE

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300 Baker Avenue
Concord, MA 01742

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410496

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report summarizes the work done on the design, construction and test of an Offset Local Oscillator for use with the Tracking Servobridge Detector as part of a system for precision bridge-type measurements on quartz crystal resonators.

The primary requirement for the Offset LO is to accept a generator input signal over the range of 0.8 to 220 MHz and produce an output which is offset

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from the input frequency by +80 kHz. This output serves as the local oscillator signal for a sensitive heterodyne detector and must be essentially free of direct generator input component to avoid a spurious receiver response.

The design approach used is to first produce a crude offset signal by phasing-type single-sideband techniques and then use a phase locked oscillator as an active filter to obtain the required spectral purity. The electronic circuits which implement this design are described in detail. The report contains the results of tests made on three Offset LO units. All requirements were met and a viable design was achieved.

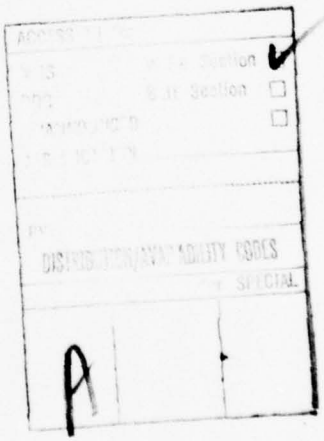
The report also contains an analysis of an electronically tunable microcircuit RF bridge suitable for the automatic measurement of quartz crystal parameters. It is concluded that the measuring system studied indeed has the potential of making the desired measurements automatically. Possible sources of errors have been analyzed and corrective solutions proposed. Expected performance is in accordance with the latest guidelines for the system.

Summary

This final technical report covers the work performed by GenRad, Inc. under Contract No. DAAB07-75-C-1341 between June 1975 and July 1976 on an Offset Local Oscillator and an electronically tunable microcircuit admittance bridge. The contract was issued in May 1975 and extended in May 1976 by the U.S. Army Electronics Command, Fort Monmouth, New Jersey. Research and development work was carried out which led to the design of two engineering models of an Offset LO covering the frequency range of 0.8 to 220 MHz.

A theoretical analysis of the behavior of an electronically tunable microcircuit bridge was performed. Although the details of a completely automatic balancing operation utilizing a tracking servobridge detector were not examined, the circuits required for automatic balancing appear realizable. The most practical method to obtain a direct readout of the resistance of the resonator under test apparently will involve digital microprocessing. In addition, the microprocessor can be used to compute other parameters such as Q or equivalent inductance. Because it does not appear possible to keep the direct accuracy of the bridge within acceptable limits throughout the entire frequency range, it may be possible with a microprocessor to make automatic corrections and to produce accurate display readouts.

The major deviations from the performance objectives expected are a reduction in the measurable resistance range at the highest frequencies, a reduction of the allowable drive level to the resonator being tested, and a limitation of the capacitance measurement accuracy at the lowest frequencies. The loss of capacitance accuracy results from the roll off of the bridge to detector coupling.



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ELECTRONICALLY TUNABLE MICROCIRCUIT BRIDGE

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LIST OF ABBREVIATIONS

AND SYMBOLS

AC	Alternating Current
AGC	Automatic Gain Control
BW	Bandwidth
dB	Decibel
dBm	Decibel Power level re 1 mW into 50Ω
Det	Detector
DSB	Double Sideband
ϵ	Symbol for small frequency increment
ECL	Emitter - Coupled Logic
ECOM	Electronics Command (U.S. Army)
f	Symbol for frequency
f_{Gen}, f_g	Symbol for Generator frequency
f_o, f_{offset}	Symbol for Offset frequency
Gen	Generator - the input to the Offset Local Oscillator
GR	General Radio, GenRad
HF	High Frequency
HPF	High Pass Filter
IC	Integrated Circuit
IF	Intermediate Frequency
IM	Intermodulation
K_a	Symbol for Amplifier transfer function
K_ϕ	Symbol for Phase detector transfer function
K_v	Symbol for Varactor tuning transfer function
LF	Low Frequency
LO	Local Oscillator
LP	Low Pass
LPF	Low Pass Filter
MHF	Medium High Frequency
MLF	Medium Low Frequency
N	Symbol for an integer number
OSLO	Offset Local Oscillator
Ø-F	Phase-Frequency
PIN	Type of RF attenuator diode

List of Abbreviations and Symbols (continued)

ppm	Parts per million
RC	Resistance - Capacitance
RF	Radio Frequency
RFI	Radio Frequency Interference
SSB	Single Sideband
SMA	Type of coaxial connector
S/N	Serial Number
Spur	Spurious
TSBD	Tracking Servo Bridge Detector
TTL	Transistor - Transistor Logic
VCO	Voltage Controlled Oscillator

Section I

OFFSET LOCAL OSCILLATOR

1. INTRODUCTION

1.1 Objectives

The Tracking Servo Bridge Detector recently developed for measuring quartz crystals requires a local oscillator signal which is offset by exactly +80 kHz from a generator frequency over the range of 0.8 to 220 MHz. This report presents the results of a development program to design and produce two engineering models of an Offset LO unit for this application. The design principles are discussed, circuit and packaging concepts described and test data is presented. The development of the Tracking Servo Bridge Detector was previously carried out under Contract DAAB 05-73-C-0609.

1.2 General Requirements

The purpose of the Offset LO unit is to produce a signal offset by +80 kHz from a generator input for use as the local oscillator in the receiver section of the Tracking Servo Bridge Detector. The receiver input mixer then will produce a constant 80 kHz IF frequency as the generator varies over the 0.8 to 220 MHz range.

It is vital that the Offset LO signal be free of spurious frequency components which result in any 80 kHz IF signal in the absence of receiver RF input. Any such spurious response limits the ability of the receiver to detect and lock to the correct bridge balance condition. The ideal situation exists when the receiver detectivity is limited only by noise.

The use of a very well balanced mixer at the receiver input results in about 50 dB of LO isolation. This eases the requirement for LO spectral purity, but it is still very stringent.

The noise level of the receiver (random fluctuations of the synchronous detector meters) corresponds to an RF input level of about -153 dBm. The LO drive to the mixer is +7 dBm. With 50 dB of mixer isolation the spurious generator component on the LO signal must be 110 dB down to be no more than the noise.

1.2 General Requirements (continued)

There are other possibilities for spurious responses besides an LO component at the f_{Gen} frequency. A (f_{Gen} + 160 kHz) spurious LO component is equally critical. So is a spurious generator component at that frequency - the receiver image response. Another more subtle possibility is the combination of an LO spurious component which combines with a generator spurious component to produce an 80 kHz IF signal. It is not sufficient to simply insure the absence of +80 kHz sidebands on the LO signal; any LO spur can potentially result in a false receiver response in combination with a certain generator spur.

Since the generator is a frequency synthesizer and the output signal is passed through a bridge which, at null, reduces the main f_{Gen} component by perhaps 80 dB, the relative level of the inevitable synthesis spurious products usually are greatly increased. This situation is particularly bad because it is difficult to predict the particular frequencies and levels of these receiver spurious responses. An 80 dB down spurious level is a typical specification for a high quality state-of-the-art synthesizer which covers the required frequency range.

The design goal for the Offset LO should, therefore, be an output with no spurious components less than 110 dB down.

A summary of the effects of spurious components on the performance of the Tracking Servo Bridge Detector System is shown in Figure 1.1.

Noise sidebands on the LO signal must also be considered. LO noise sidebands at ±80 kHz add to the receiver noise and should be below the -110 dB relative level established for discrete spurious components, measured in the post detection bandwidth of a few Hz. LO noise sidebands close to the main component can also contribute to receiver noise. The isolation of the input mixer makes these sidebands relatively unimportant compared to those of the generator signal itself. The receiver IF bandwidth is 2 kHz and, therefore, it is the noise sidebands out to about ±2 kHz from the LO carrier which are of interest. This establishes the loop bandwidth that is desirable in any phase-locked oscillators that are used.

SUMMARY OF TSBD/OSLO SPURIOUS RESPONSES

Case	Gen Pure	LO Pure	Comments
1	Yes	Yes	The only spurious response is leakage of generator signal into receiver input.
2	No	Yes	The receiver has no RF selectivity so a generator spur at the image frequency f_{Gen} +160 kHz would produce a spurious response. Spurious level set by synthesizer specs and ratio is enhanced by bridge balance. Other synthesizer spurs can produce responses caused by harmonic intermodulation products in receiver mixer.
3	Yes	No	Feedthrough of generator signal into the LO output makes a leakage signal. An LO component at f_{Gen} +160 kHz could also. No other possible LO spur can, by itself, cause a false response.
4	No	No	The combination of any two spurs with 80 kHz separation can cause a false response (or any such harmonic intermodulation). The level of any such possibility is set by synthesizer specs and the ratio is enhanced by bridge balance.

FIGURE 1.1

1.2 General Requirements (continued)

The Offset LO has to operate over the entire frequency range of the Tracking Servo Bridge Detector. Range switching is permissible, but wideband techniques are desirable where practical to reduce cost and complexity.

The offset accuracy is dictated by the synchronous detector reference crystal oscillator lock range in the Tracking Servo Bridge Detector. An accuracy of ±50 ppm is acceptable.

Input and output levels are dictated by those specified for the Tracking Servo Bridge Detector: 0 dBm generator input and +10 dBm LO output. The Offset LO unit will obtain power and certain control and alarm signals from the Tracking Servo Bridge Detector. It is to be housed in a separate bench/rack package with as low a height as possible.

1.3 Goal Specification

These factors thus lead to the following list of tentative specifications for the Offset LO unit for the Tracking Servo Bridge Detector system. These specifications served as goals for the development work and some changes are necessary based on the actual test results described later.

Frequency Range: 0.8 to 220 MHz

Range Switching: as follows -

No.	MHz
1	125-220
2	75-140
3	45-85
4	28-52
5	17-32
6	11-20
7	7-13
8	5-9

1.3 Goal Specifications (continued)

No.	MHz
9	3.2-6
10	2. -3.7
11	1.3-2.3
12	0.8-1.5

Frequency Offset: +80 kHz ±50 ppm with respect to generator input

Generator Input: 0 dBm nominal into 50Ω

Offset LO Output: +10 dBm ±1 dB into 50Ω

Spurious Output Components: All non-harmonically related components ≥ 110 dB down. This applies to all discrete components and noise components at ±80 kHz from the carrier measured in a 1 Hz bandwidth.

Output Harmonic Distortion: ≥ 25 dB down

Power Supplies: -5.2V at 0.7A max
-22V at 0.2A max
-18V at 0.2A max
+18V at 0.2A max

Interface Signals: Range information and unlock alarm compatible with Tracking Servo Bridge Detector.

Package: Rack/Bench unit similar to Tracking Servo Bridge Detector with minimum height and blank panel.

2. BLOCK DIAGRAM

The generation of a signal slightly offset from another over a wide frequency range becomes a challenging job when stringent demands are placed on the spectral purity of the offset output. The approach taken in this design, based on the results of a study of several alternatives in 1974[1], first generates a crude offset signal by phasing type single sideband (SSB) techniques and then uses a phase locked loop as a filter to achieve the required spectral purity. A basic block diagram of the method is shown in Figure 2.1.

Generation of the SSB offset reference signal is done at half-frequency in order to reduce the spurious generator component on the LO output and to permit the use of digital techniques for RF quadrature generation.

The LO output comes from one of twelve band switched voltage controlled oscillators (VCO's) which is phase locked to the offset reference. In order for the lock loop to serve as an effective filter to remove spurious output components several requirements must be met:

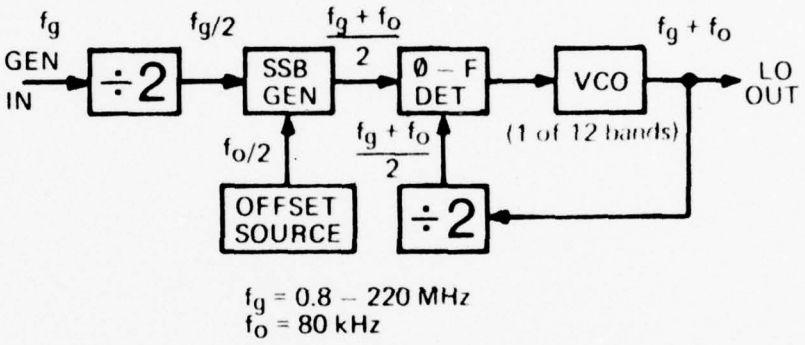
(1) Modulation of the VCO via the varactor control line must be reduced by a loop filter.
(2) Modulation of the VCO via reverse transmission from the VCO input to the phase detector must be reduced by an isolation amplifier.
(3) Coupling via power supply lines must be reduced by effective filtration.
(4) Coupling via radiation must be reduced by effective shield enclosures.

A more complete block diagram of the Offset LO unit is shown in Figure 2.2. There are three separately enclosed modules: (1) VCO (2) Lock-Loop and (3) Low Pass Filter.

---

(1) Riley, William J., "Design Study For A Frequency Offset Generator", Final Report on ECOM Contract No. DAAB07-74-C-010, General Radio Company, Bolton, Mass., 24 August 1974

OFFSET LO BASIC BLOCK DIAGRAM



f_g = 0.8 – 220 MHz
f_o = 80 kHz

FIGURE 2.1

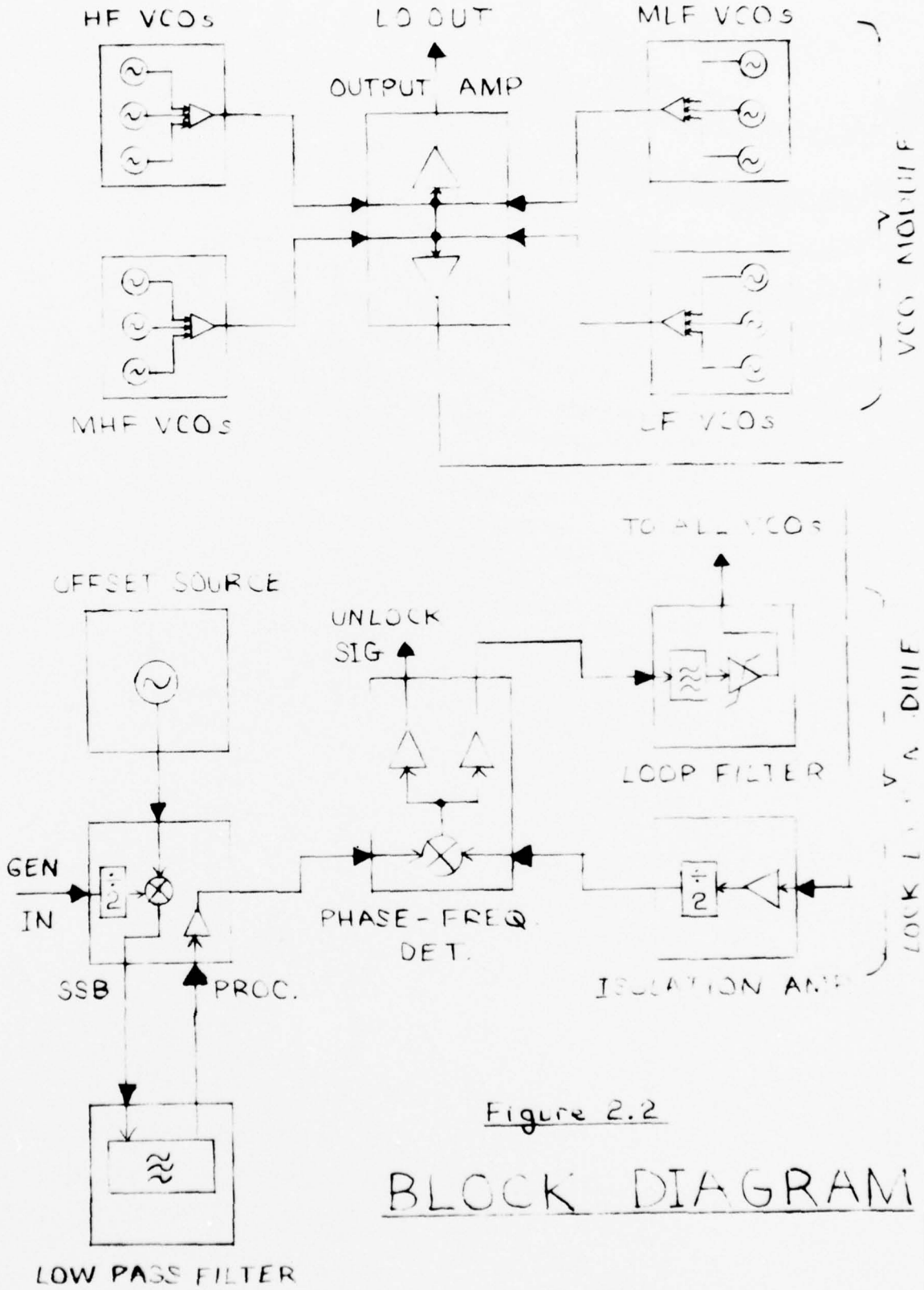


Figure 2.2

BLOCK DIAGRAM

Block Diagram (continued)

The VCO module contains five sections, four VCO boards, each holding three VCO's and one Output Amplifier board.

The Lock-Loop module also contains five sections. These are:

(1) The Offset Source board which generates the 40 kHz half-offset signal.

(2) The SSB Processor board which accepts generator and offset inputs to produce the reference signal for the lock loop.

(3) The Isolation Amplifier board which provides a VCO sample for the lock loop.

(4) A Phase-Frequency Detector board.

(5) A Loop Filter board.

The Low Pass Filter module is a single section which contains six switched filters necessary for proper lock loop operation on the lower frequency ranges.

The individual sections are described in more detail in the following pages.

3. CIRCUIT DESCRIPTION

3.1 Voltage Controlled Oscillators

The LO output signal is generated by a series of twelve voltage controlled oscillators (VCO's) which cover the frequency range between 0.8 and 220 MHz. Each VCO has a tuning ratio of about 1.85:1 and adjacent ranges have at least 10% overlap. The exact frequency ranges are part of the specifications for the Tracking Servo Bridge Detector. The VCO's are packaged on four etched circuit boards, each containing three VCO's and one associated summing amplifier.

The same basic VCO circuit is used for the nine highest frequency ranges and is shown in Figure 3.1.1.

The circuit is a grounded base amplifier with positive feedback from collector to emitter. The impedance step down in the feedback path, a necessary condition for oscillation, is accomplished by tapping off at the junction of the two series-connected tuning varactors. Alternate methods, such as link coupling, an inductive tap or a separate capacitive divider are less satisfactory at high frequencies where leakage reactance is troublesome and additional shunt capacitance limits the tuning range.

A series of hyper-abrupt tuning varactors are used which can achieve tuning ratios well over 2:1. In practice the varactor voltage range is restricted to limit the frequency range to only slightly more than the already overlapping nominal ranges to avoid extreme changes in the slope of the varactor tuning characteristic. A series of powdered iron toroidal cores are used as tank coils.

Low harmonic distortion is obtained without impractical low pass filters by the use of an automatic gain control (AGC) loop which senses the LO output level and varies the oscillator loop gain by means of a PIN diode attenuator network.

The three low frequency VCO's have the basic circuit configuration shown in Figure 3.1.2. They differ from the other VCO's only in that the feedback is taken from a tap in the tank coil. This

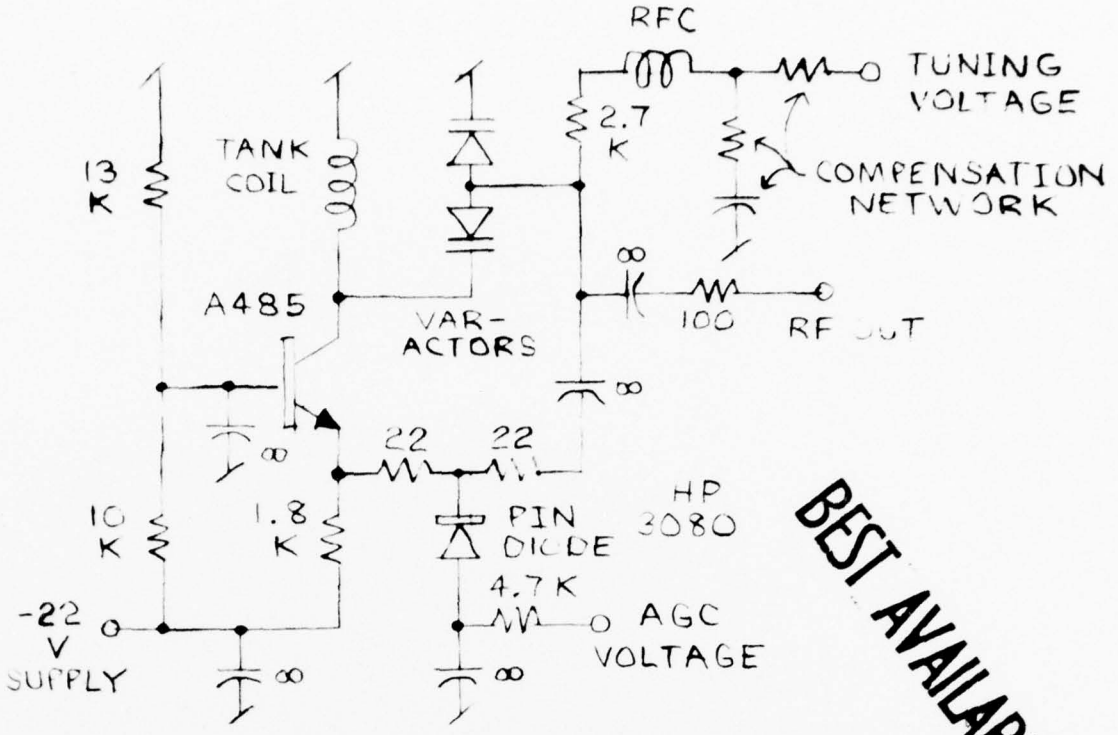


Fig. 3.1.1. HF VCO

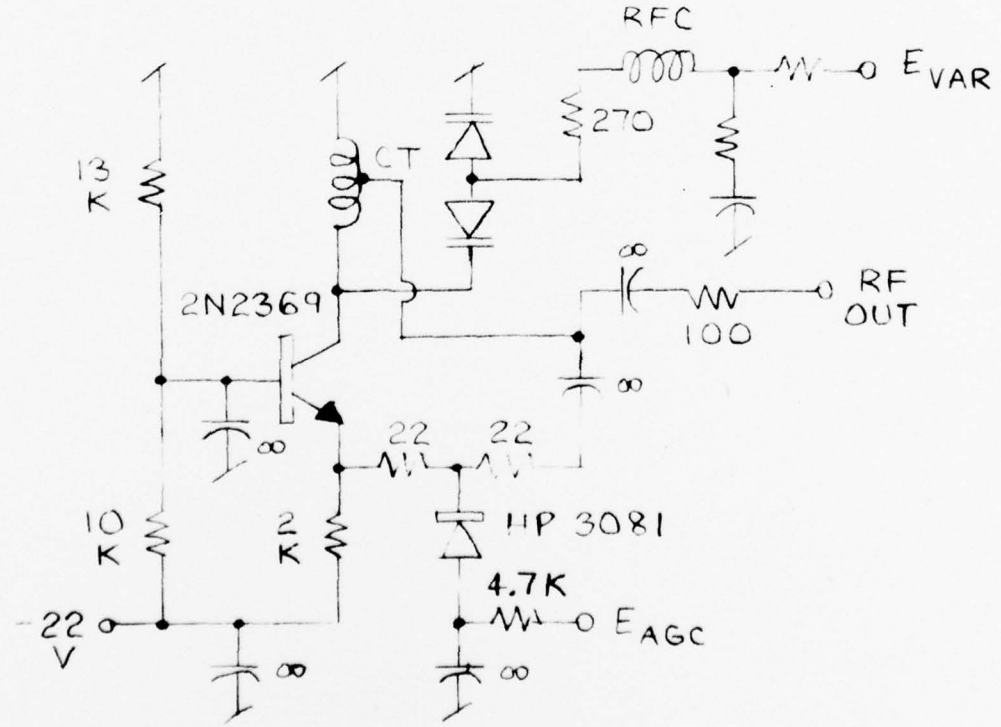


Fig. 3.1.2. LF VCO

configuration is better at the lower frequencies where leakage reactance is not a problem, but the RC low pass network caused by large coupling capacitors on the varactor control line would add excessive phase lag which would make the lock loop stabilization more difficult.

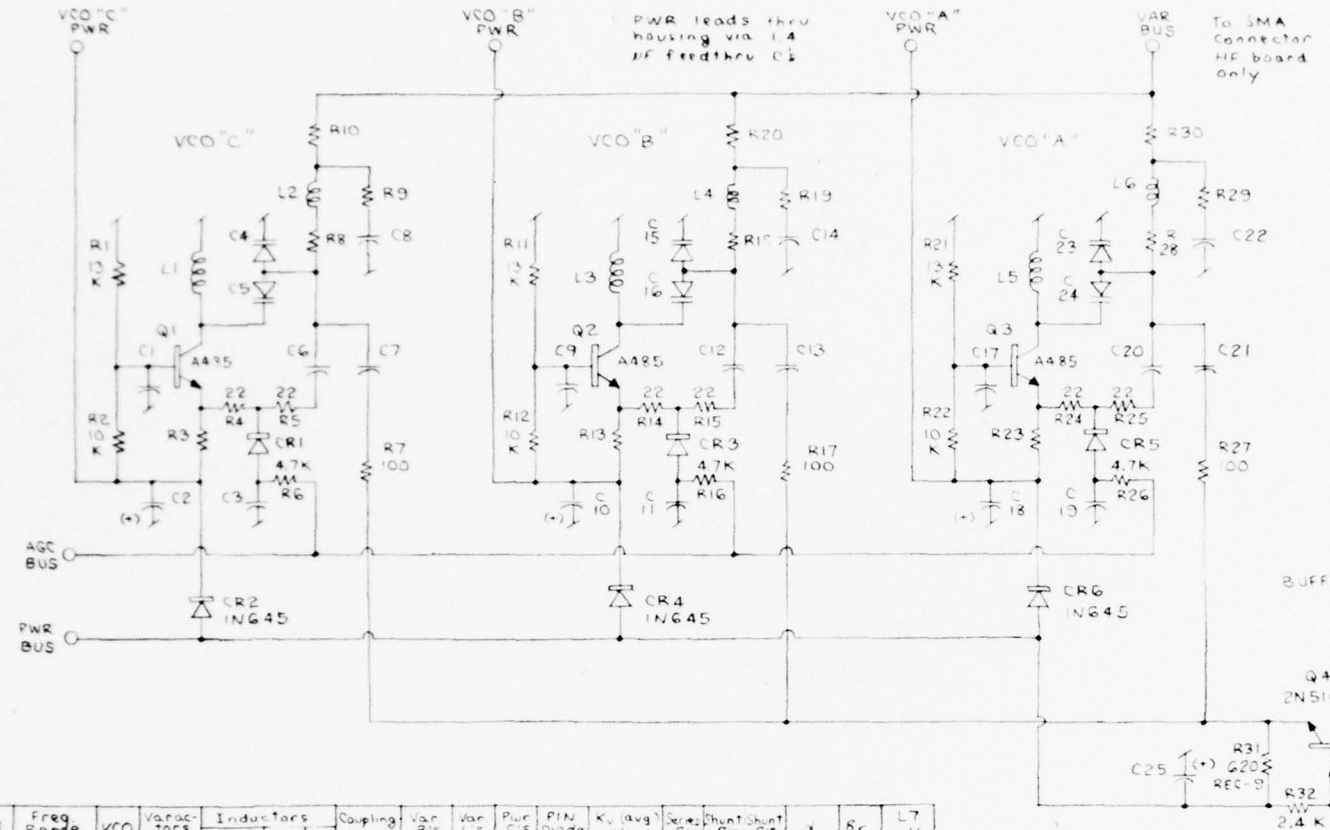
The wide overall frequency range ($\simeq$ 300:1) and corresponding change in varactor tuning sensitivity has a great impact on the lock loop, of course. A passive compensation network is associated with each VCO to permit lock loop servo stability and will be discussed in detail in Section 3.8.

The varactor tuning characteristic is also compensated for by a nonlinear loop amplifier as discussed in detail in Section 3.8.

Each of the four VCO boards also has a grounded base summing amplifier which combines the three VCO outputs, only one of which can be active, into a single output.

VCO switching is accomplished simply by applying -22V only to the desired oscillator. A diode network also applies power to the corresponding summing amplifier.

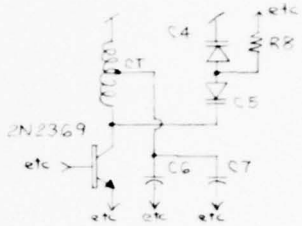
The circuit schematic for the four complete VCO sections is shown in Figure 3.1.3.



VCO BOARD

E6835 WJR 9/23/75
Rev 10/1/75
7/26/76

Ckt for LF Ranges:



Board	Freq Range, MHz	VCO	Varactors KV_01	Inductors Core	N	#	Coupling Cs, μF	Var R's KΩ	Var L's μH	Pwr C's μF	PIN Diode HPA	K_v (avg) rad/s/V	Series R's KΩ	Shunt R's Ω	Shunt C's μF	X	R_E KΩ	L7 μH
HF	125-220	A	22	T-30-0	6	24	.001	2.7	.33	.01	3080	7×10^7	100	91	2.2	1100	1.0	
2995 4179	75-140	B	23	T-30-0	7	24	.001	2.7	.82	.01	3080	5.5×10^7	68	120	1.5	568	1.1	.82
	45-85	C	23	T-30-12	10	24	.001	2.7	1.5	.01	3080	3.5×10^7	82	180	1.0	457	1.8	
MHF	28-52	A	24	T-30-10	11	24	.001	2.7	3.9	.01	3080	2×10^7	62	330	47	189	1.8	
2995 4180	17-32	B	24	T-30-10	20	27	.001	2.7	8.2	.01	3080	1.5×10^7	47	430	47	100	1.8	4.7
	11-20	C	25	T-30-6	25	27	.001	2.7	22	.01	3080	1×10^7	47	620	.22	77	1.8	
MLF	7-13	A	25	T-30-6	36	28	.0047	470	47	.1	3080	5×10^6	62	1.3K	.22	48.7	1.8	
2995 4181	5-9	B	25	T-30-2	45	31	.0047	470	120	.1	3080	3×10^6	30	1.1K	.22	29.3	1.8	22
	3.2-6	C	26	T-30-1	45	31	.0047	470	330	.1	3080	1.5×10^6	62	2.2K	.22	29.2	1.8	
LF	2-3.7	A	26	266T 125 3D3	24 CT	28	.01	270	680	1.0	3081	1×10^6	36	3.3K	.05	11.9	1.8	
2995 4182	1.3-2.3	B	26	266T 125 3D3	34 CT	28	.01	270	1000	1.0	3081	6×10^5	12	3.3K	.05	4.6	1.8	39
	0.8-1.5	C	26	266T 125 3D3	22 CT	28	.01	270	1500	1.0	3081	2×10^5	3.3	3.3K	.05	2.0	1.8	

Notes:
Varactors are C4,5 C15,16 & C23,24
Inductors are L1 L3 & L5
Coupling Cs are C1,C3 C6,C7 C9,C11 C12,C13 C17,C19 & C26 C20,C21 & C27
Var R's are R8 R18 & R28
Var L's are L2 L4 & L6
Pwr C's are C2 C10 C18 & C25
PIN diodes are: CR1 CR3 & CR5
K_v (avg) meas from Evar = 4 to 10V w/o non-linear dc amp
Series R's are R10 R20 & R30
Shunt R's are R9 R19 & R29
Shunt C's are C8 C14 & C22
R_E's are R3 R13 & R23
use REC-9

$\alpha = \frac{R_{10}+R_9}{R_9}$, etc.

Note: Consult Parts Lists for exact component information

FIGURE 3.1.3 VCO BOARD

3.2 Output Amplifier

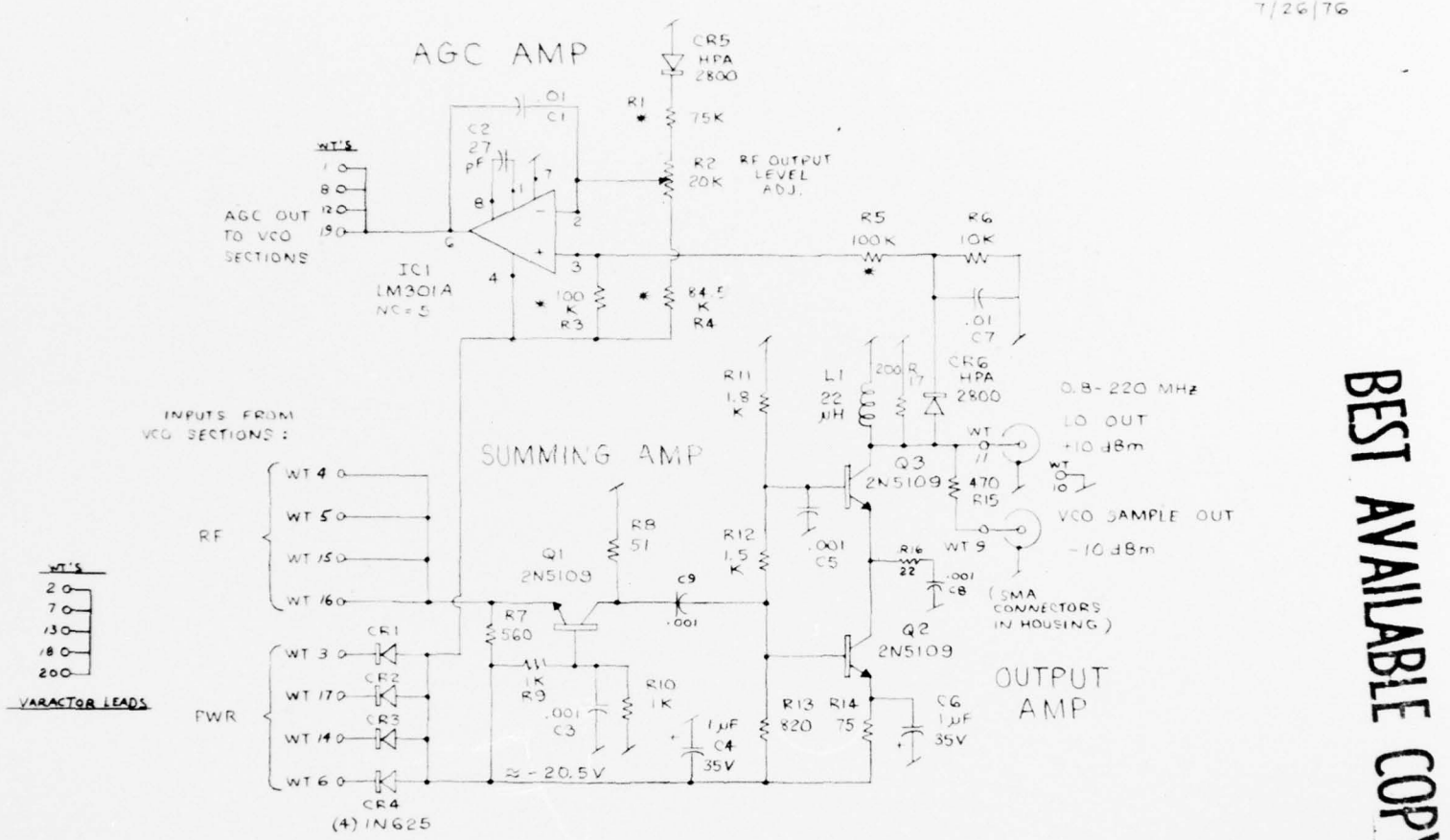
It is the function of the Output Amplifier section to accept the signal from the selected VCO and provide a +10 dBm LO output for the Tracking Servo Bridge Detector. An additional output at -10 dBm provides the VCO sample signal for the lock loop.

Figure 3.2 shows the circuit schematic for this section. A grounded base summing amplifier combines the outputs from the four VCO sections (only one of which is active) and drives a cascode output stage. A diode detector samples the main output, producing a dc voltage which is compared with a reference level by an operational amplifier. This device provides an output which drives a PIN diode attenuator in the VCO circuit, maintaining a constant output level and reducing harmonic distortion.

The Output Amplifier section is powered by a diode network from the active VCO section.

OUTPUT AMPLIFIER SECTION

E6835
WJR
9/25/75
REV 10-14-75 BLD
7/26/76



All resistors REC-9 except * = REF-60 # R2 = POSW-8 6058-3205

27 pF 4400-6484 .001 4400-6422 HPA-2800 6082-1034

.01 4400-6351 1 µF, 35V See 4450-1W-2 2N5109 8210-1198

FIGURE 3.2 OUTPUT AMPLIFIER

3.3 Isolation Amplifier

The Isolation Amplifier section provides a signal at $f_{LO}/2$ to the Phase-Frequency Detector section which serves as a sample of the VCO for the lock loop. Since the lock loop operates at half frequency, this section must contain a binary divider. It is also necessary that there be sufficient reverse isolation from the Ø-F Detector into the VCO so that the effectiveness of the lock loop as a filter will not be limited by the presence signals (such as f_{Gen}) via this path.

Figure 3.3 shows the circuit schematic of the Isolation amplifier section. A cascode amplifier, a configuration having high reverse isolation, accepts the -10 dBm VCO sample signal and drives a Schmitt Trigger which provides an ECL waveform for the binary divider. This section uses both the -22V and -5.2V supplies.

ISOLATION AMPLIFIER & ÷2 SECTION

E-6835
7/14/75
WJR

ECO 8-18-75 RLD
7/26/76

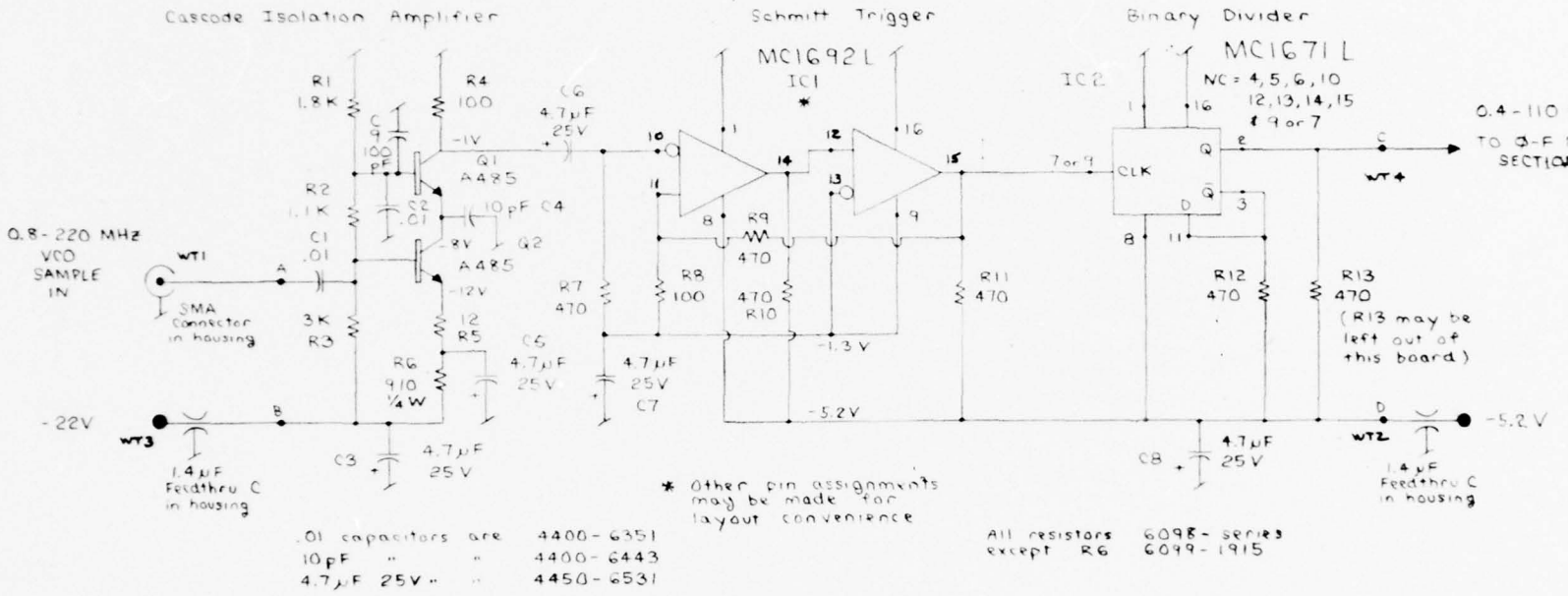


FIGURE 3.3 ISOLATION AMPLIFIER

3.4 Offset Source

Generation of the 40 kHz offset signal begins with a crystal oscillator at 1280 kHz. After division by 32 the resulting 40 kHz square wave is applied to a quadrature bandpass filter to produce the required sine wave signals with 90° phase difference. Low harmonic distortion is necessary to reduce spurious components on the LO output.

Figure 3.4 shows the circuit schematic of the Offset Source Section. The quadrature bandpass filter consists of three op amps. Two are integrators and the third is an inverter. Without the 100 kΩ resistors across the integrating capacitors the circuit would oscillate at a frequency where the loop gain is unity. The loop phase shift would always be 180° through the two integrators and 360° overall. The frequency of oscillation would be set by the loop amplitude condition via a variable resistor.

When the 100 kΩ resistors are added to the integrators they can no longer produce a full 180° phase shift and the loop can no longer oscillate. The circuit becomes an active filter with a Q factor set by the integrator feedback resistors. The 100 kΩ resistors result in a Q around 50. The two outputs are still very nearly in phase quadrature. Harmonic distortion is at least 40 dB down. The zener diodes across the second integrator limit the signal amplitude under transient conditions to insure stability.

One of the outputs is adjustable in amplitude to the condition which results in best suppression of the lower sideband.

An on-board IC voltage regulator provides ±15V from the preregulated ±18V input.

The frequency stability of the offset is specified as within ±50 ppm, sufficient to insure lock up of the IF reference oscillator in the Tracking Servo Bridge Detector.

OFFSET SOURCE SECTION 7-30-75 E-6835 WJR

Rev 2/26/76
7/26/76

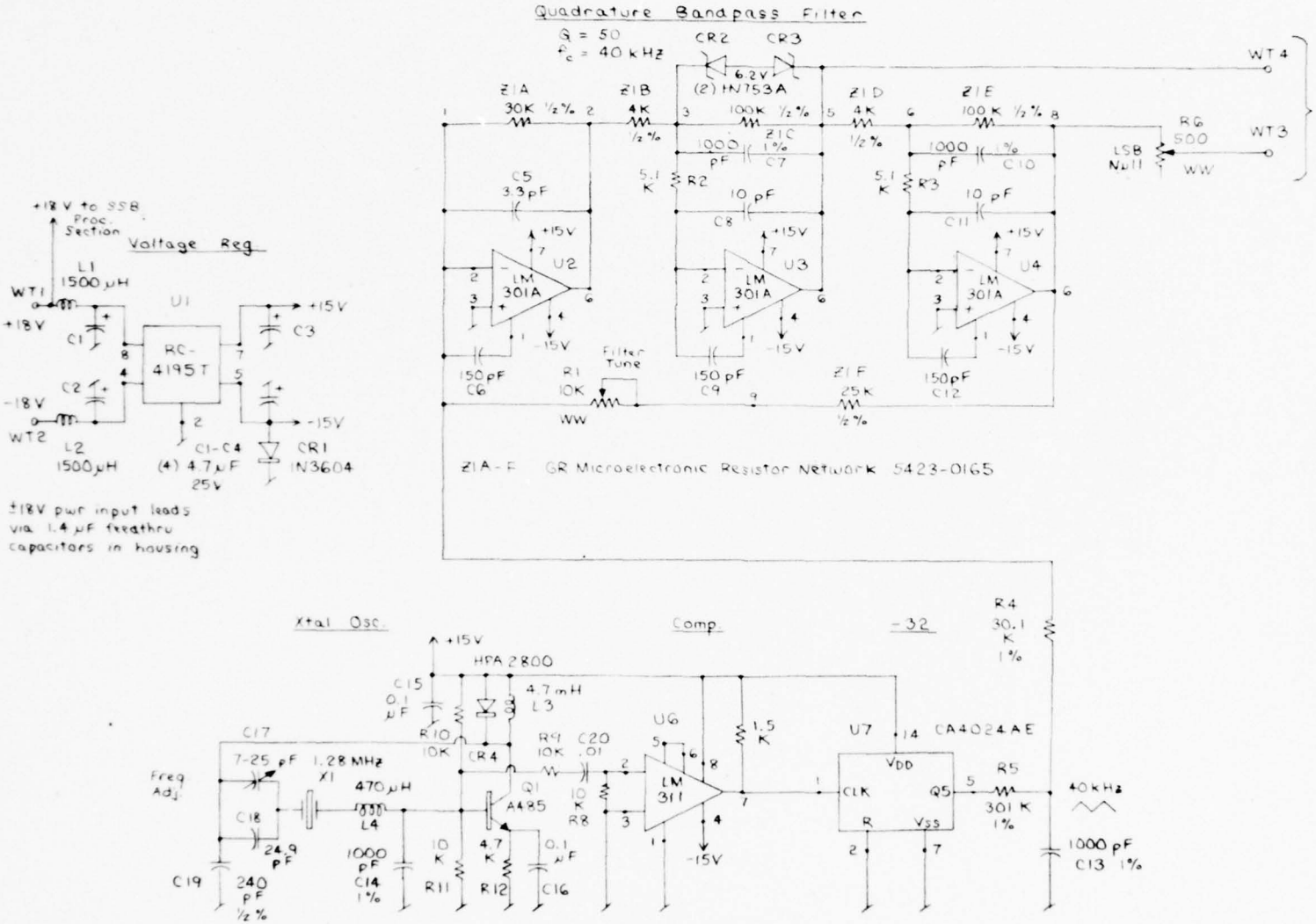


FIGURE 3.4 OFFSET SOURCE

3.5 SSB Processor

Generation of the precise +80 kHz offset required for the local oscillator signal is accomplished over a greater than 8 octave range by a digital-phasing type SSB processor. Quadrature signals are produced at both the offset and Gen frequencies and a pair of mixers generate DSB signals which are summed to produce a SSB offset reference signal for the VCO phase lock loop. It is a relatively simple matter to produce quadrature signals at the fixed offset frequency, but conventional quadrature hybrids or other 90° phase difference networks cannot cover the 275:1 RF frequency range without switching. The use of digital techniques provides a wideband approach which is simpler and less costly.

SSB processing is actually done at half-frequency. Not only does this make practical the digital implementation of the SSB processor and Phase-Frequency Detector by reducing the maximum RF frequency to 110 MHz, but also, by changing the offset to 40 kHz, greatly reduces the level of 80 kHz sidebands on the Offset LO output.

The required half-frequency RF quadrature signals are produced as shown in Figure 3.5.1. The differential outputs of a high speed ECL line receiver are used to clock two flip-flops. The flip-flop outputs are, therefore, half-frequency quadrature signals. The flip-flops are interconnected so as to always produce the same relative output phasing.

It was originally intended to extend the use of digital techniques by using Exclusive-OR gates as balanced mixers as was done in the demonstration LO unit. It was recognized, however, that there were potential difficulties with both balance stability and offset frequency harmonics. In particular, spurious sidebands were produced as mixing products between the desired $(f_{Gen} + f_{offset})/2$ and harmonics of $f_{offset}/2$ which can lie arbitrarily close to the desired line and, therefore, cannot be filtered by the lock loop.

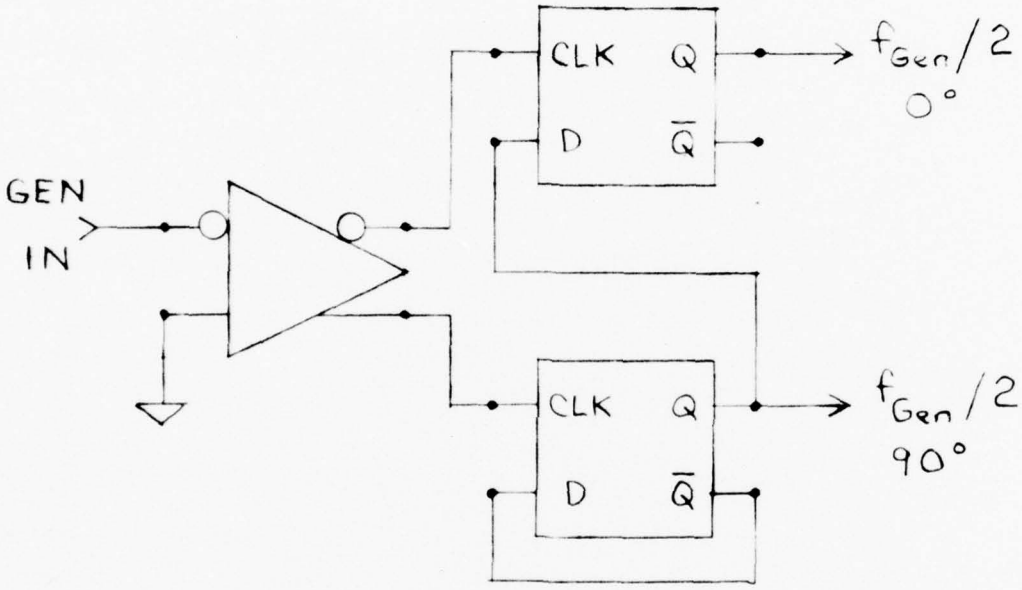


Fig. 3.5.1.

RF Quadrature Generation

3.5 SSB Processor (continued)

This problem, as well as the large third order IM levels of the digital mixers, was solved in the 37 - 85 MHz demonstration unit by using small amplitude sine wave offset drive signals. That solution was not only inadequate for the low frequency ranges, but also compromised carrier balance at the high frequency end, and, therefore, another configuration was devised.

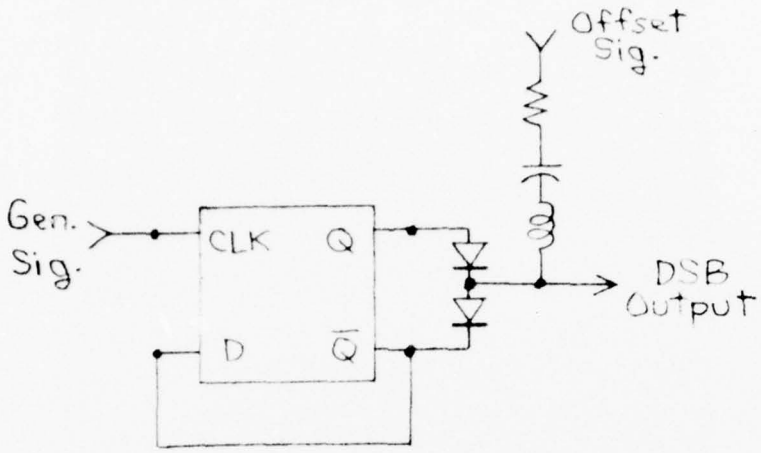
The single-balanced mixer configuration shown in Figure 3.5.2 was found to give better results. It is extremely simple and interfaces directly to the ECL devices. A pair of series connected low offset hot carrier diodes is connected between the two complementary ECL outputs and the offset sine wave is applied to the junction of the diodes. The output is, for alternate half-cycles of the RF, either the offset signal biased at the ECL reference level or simply the dc level. The output spectrum is a DSB suppressed carrier signal, plus the offset signal. Figure 3.5.3 shows the spectrum of the DSB mixer output at 0.8, 10 and 220 MHz.

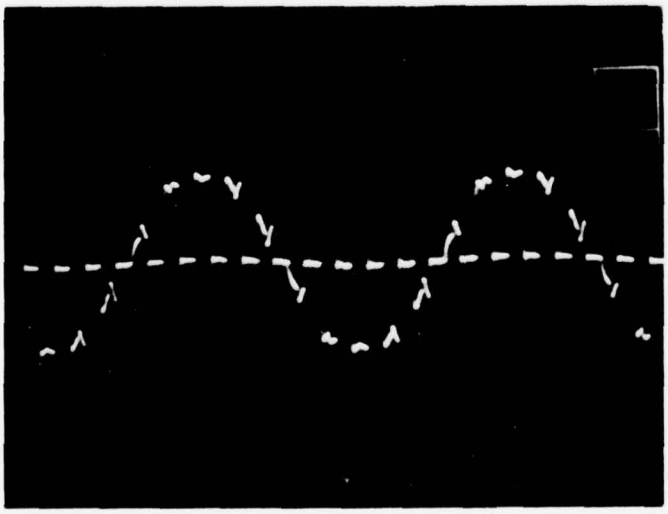
The outputs of the two quadrature paths are summed (actually differenced) by a hybrid transformer combiner and the offset signal component is removed by a high pass filter. The resulting SSB signal is the desired reference signal for the phase lock loop. Figure 3.5.4 shows the spectrum of the SSB reference signal at 0.8, 10 and 220 MHz.

It is necessary to convert the SSB reference signal into an ECL waveform for the Phase-Frequency detector and this is accomplished by an AM685 comparator. Unfortunately, any comparator or limiter is also effectively a mixer. It is necessary to low pass filter the SSB reference signal ahead of the comparator to avoid spurious mixing products.

Serious difficulties can arise from the odd harmonics of the squarewave RF signal. The spectrum of the SSB signal at the output of the hybrid combiner is shown in Figure 3.5.5. The desired component is at $(f + \epsilon)$, while a strong $(3f - \epsilon)$ component

DSB MIXER





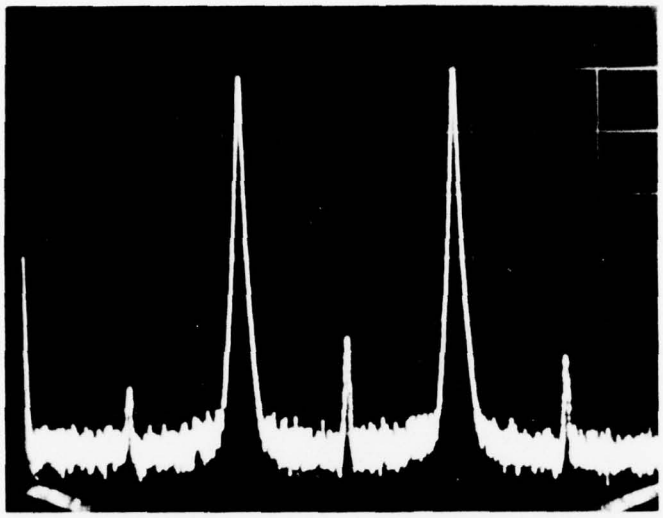
Mixer Output
Waveform

f_{Gen} = 800 kHz
2 μsec/cm horiz
0.5V/cm vert

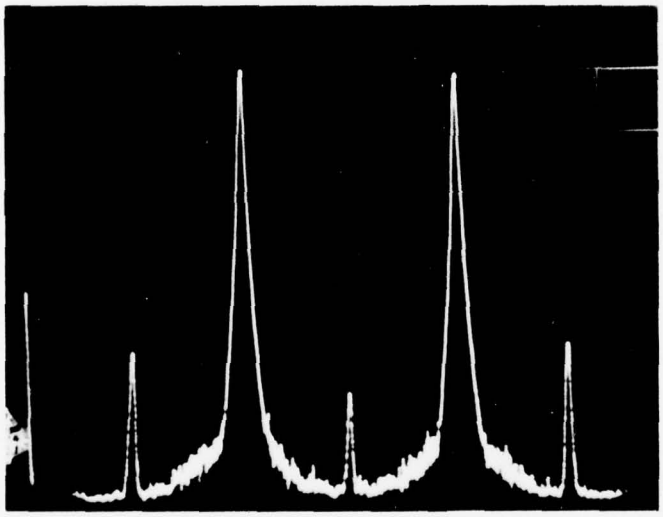
FIGURE 3.5.2

DSB MIXER SPECTRA

FIGURE 3.5.3



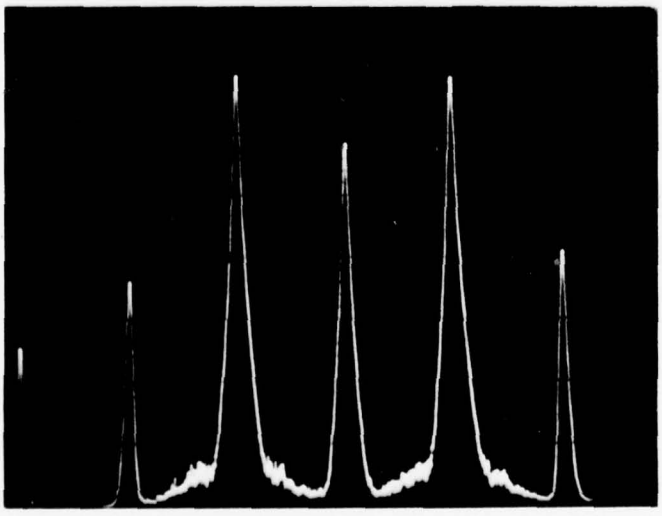
f_{Gen} = 0.8 MHz



f_{Gen} = 10 MHz

All:

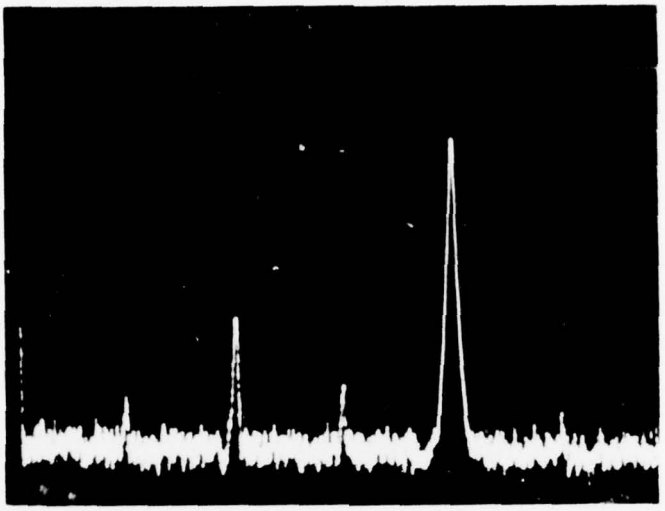
20 kHz/cm horiz
10 dB/cm vert
$f_{center} = \frac{f_{Gen}}{2}$
1 kHz RF BW
100 Hz Video BW



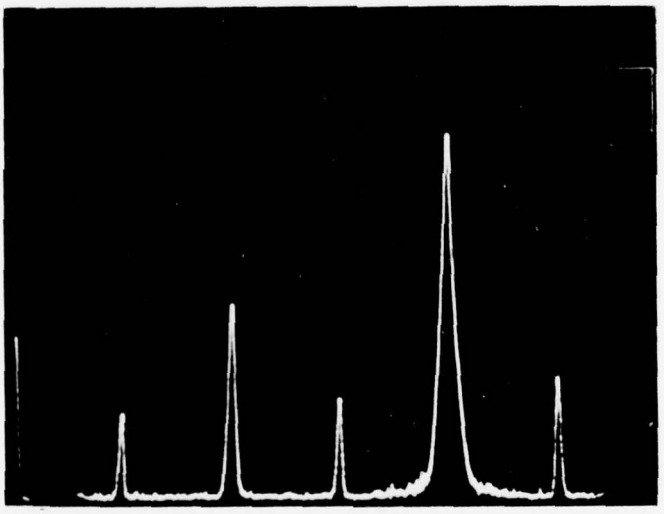
f_{Gen} = 220 MHz

FIGURE 3.5.4

SSB REF. SIG. SPECTRA
(at HPF Output)



f_{Gen} = 0.8 MHz

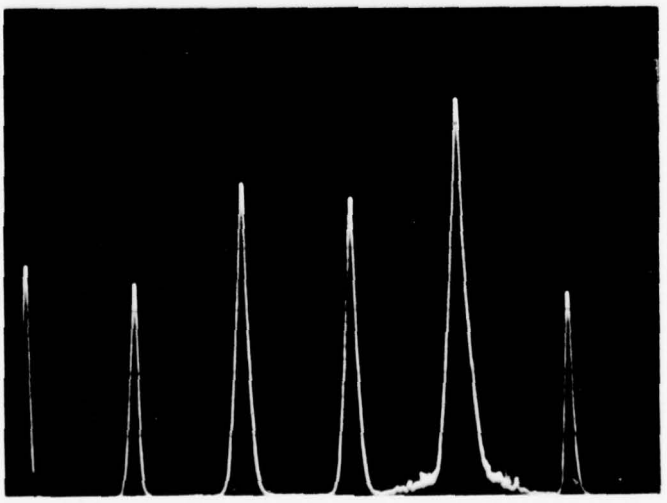


f_{Gen} = 10 MHz

All:

20 kHz/cm horiz
10 dB/cm vert
$f_{center} = \frac{f_{Gen}}{2}$

1 kHz RF BW
100 Hz Video BW



f_{Gen} = 220 MHz

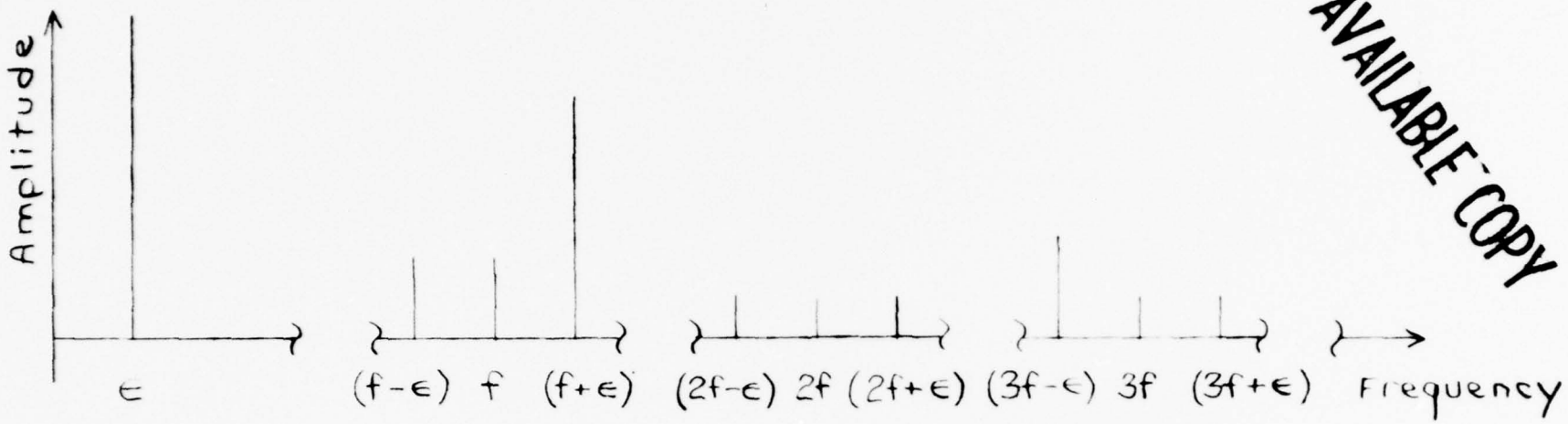


Fig. 3.5.5 SSB Spectrum

exists in the third harmonic region. If any mixing occurs in a subsequent stage a third order IM term $(3f - \epsilon) - 2(f + \epsilon) = (f - 3\epsilon)$ is generated. Such mixing inevitably does occur in the comparator whichconverts the low level reference signal into an ECL waveform. Similar terms occur due to higher odd order RF harmonics. The spectrum around $(f + \epsilon)$ will contain many rather strong $\pm N\epsilon$ "pickets" which can cause enough phase jitter on the ECL reference signal that the loop cannot lock.

The desired component of the loop reference signal need only be about 10 dB stronger than any one other to obtain lock. Once in lock, the LO output spectrum is pure by virtue of careful shielding, isolation and loop filtration. However, the comparator output spectrum will contain several $\pm N\epsilon$ components only about 10 dB down at the low frequency end of the range if the SSB signal is fed directly into the comparator.

The only effective solution to this problem is a low pass filter ahead of the comparator. The SSB reference signal is, therefore, routed to the Low Pass Filter Section before reaching the comparator on the six lowest frequency ranges.

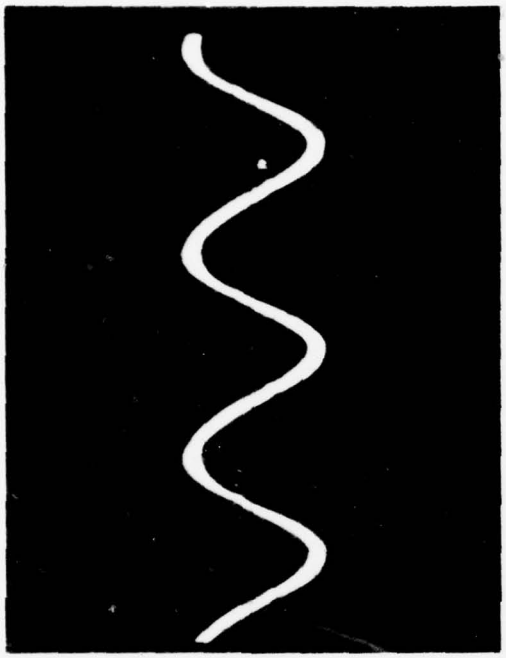
The importance of the low pass filtration is illustrated in Figure 3.5.6 through 3.5.8 which show the effect of various low pass filters on the comparator input and output signals. A generator frequency of 3.0 MHz is shown which results in a 1540 kHz SSB reference signal and normal operation on the 2-3.7 MHz range with a nominal 2 MHz LPF cut-off frequency. As successively higher cut-off filters are used the signal waveforms and spectra deteriorate and proper loop lock becomes impossible.

It was found necessary to amplify the offset reference signal ahead of the comparator. The output of the DSB mixers is limited by IM product generation. The SSB reference signal is efficiently summed by the hybrid transformer, but is attenuated by nearly 10 dB in the more complex low frequency LP filters and associated diode switching. Furthermore, it was found desirable to introduce a considerable amount of hysteresis (100 mV p-p) in the reference

REFERENCE COMPARATOR INPUT WAVEFORM
WITH VARIOUS LOW PASS FILTERS

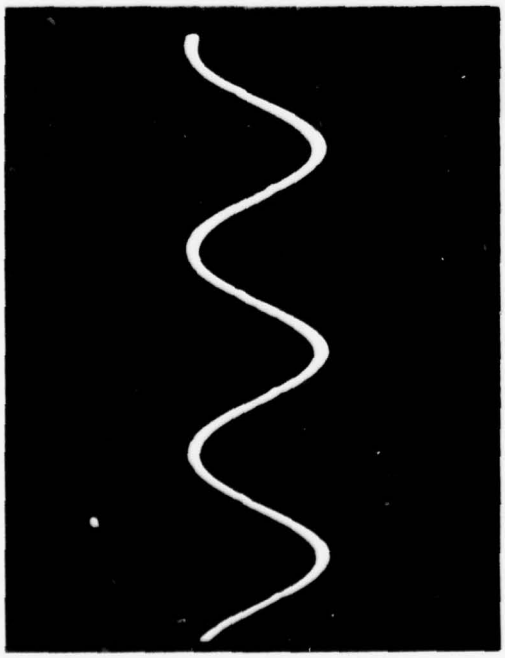
FIGURE 3.5.6

100 μsec/cm Horiz.
200 mV/cm Vert.



3.2 - 6 MHz Filter

No Filter



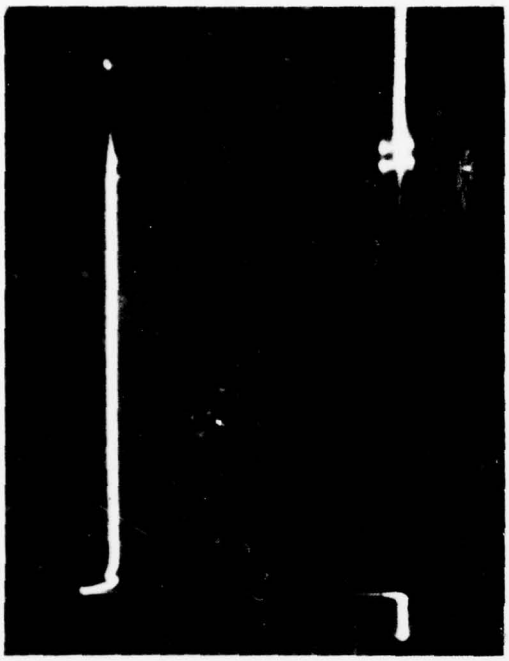
Normal Filter

5 - 9 MHz Filter

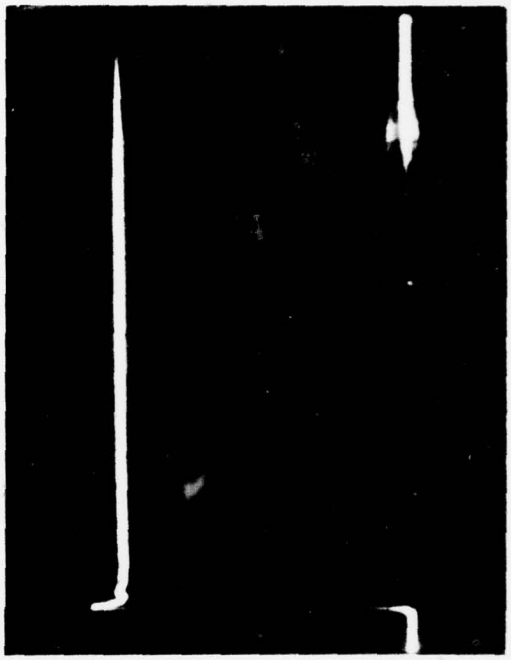
FIGURE 3.5.7

REFERENCE COMPARATOR OUTPUT WAVEFORM
WITH VARIOUS LOW PASS FILTERS

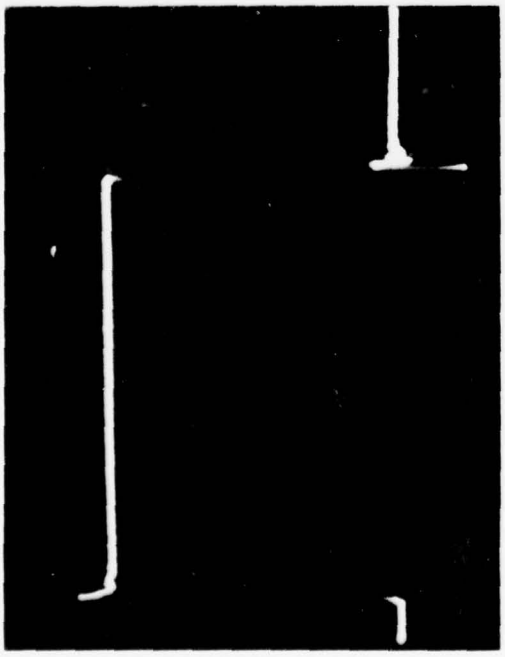
50 μsec/cm Horiz.
200 mV/cm Vert.



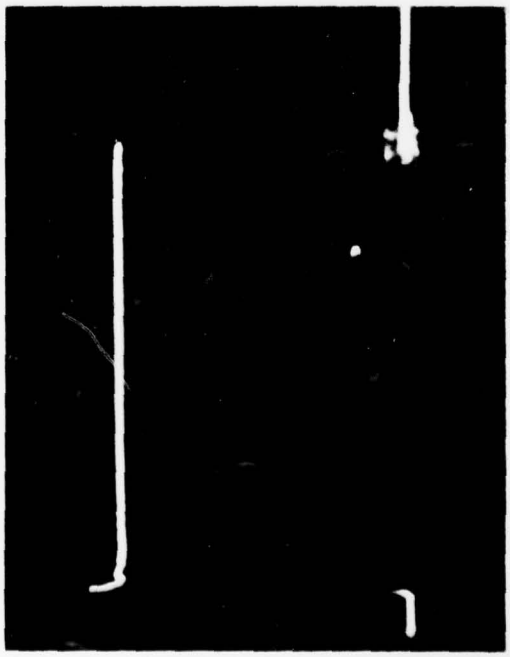
3.2 - 6 MHz Filter



No Filter



Normal Filter



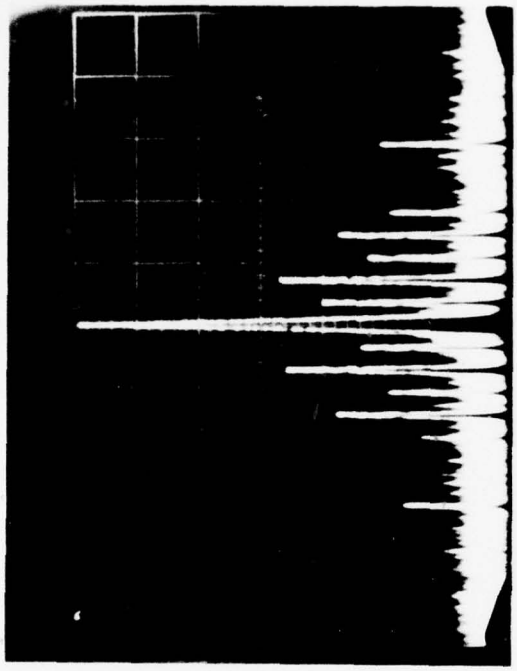
5 - 9 MHz Filter

FIGURE 3.5.8

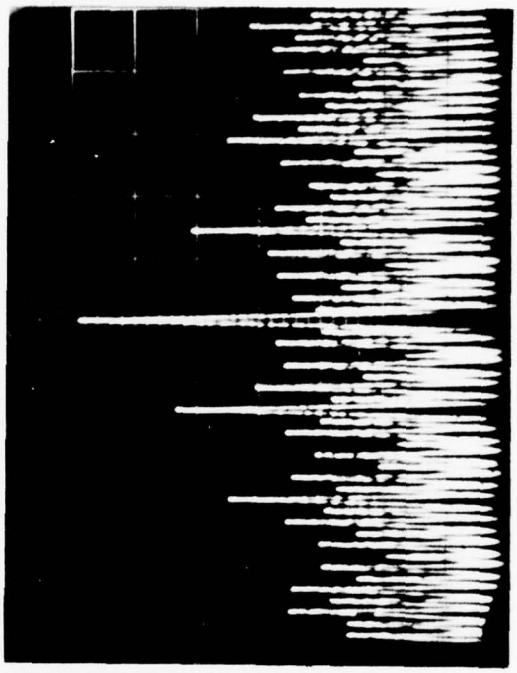
REFERENCE COMPARATOR OUTPUT SPECTRA
WITH VARIOUS LOW PASS FILTERS

f_{center} = 1540 kHz
100 kHz/cm Horiz.
10 dB/cm Vert.

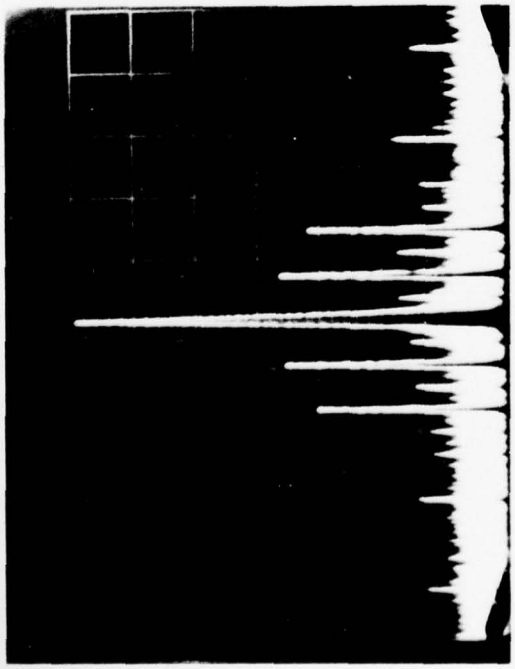
IF BW = 3kHz
No Video Filter



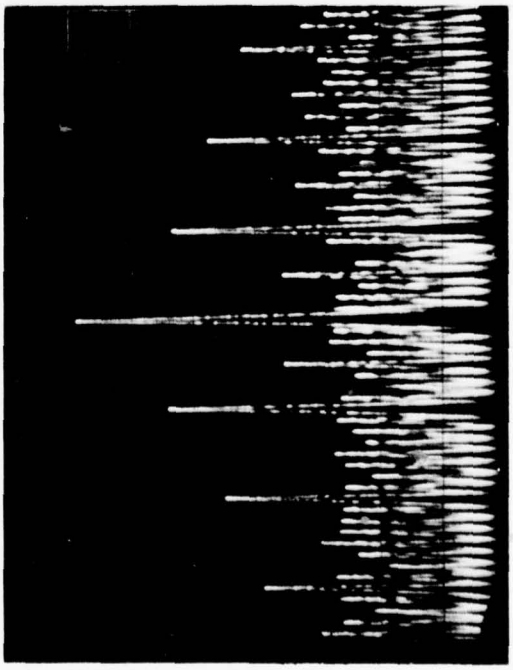
3.2 - 6 MHz Filter



No Filter



Normal Filter



5 - 9 MHz Filter

3.5 SSB Processor (continued)

comparator. Consequently, an amplifier with about X 4 gain was added ahead of the comparator. This circuit is shown in Figure 3.5.9, and is straight forward except for the PIN diode switched 100 pF capacitor at the amplifier output. This serves to restrict the bandwidth for the low frequency ranges, reducing pulsed noise pickup at the comparator input.

The schematic diagram of the complete SSB processor is shown in Figure 3.5.10.

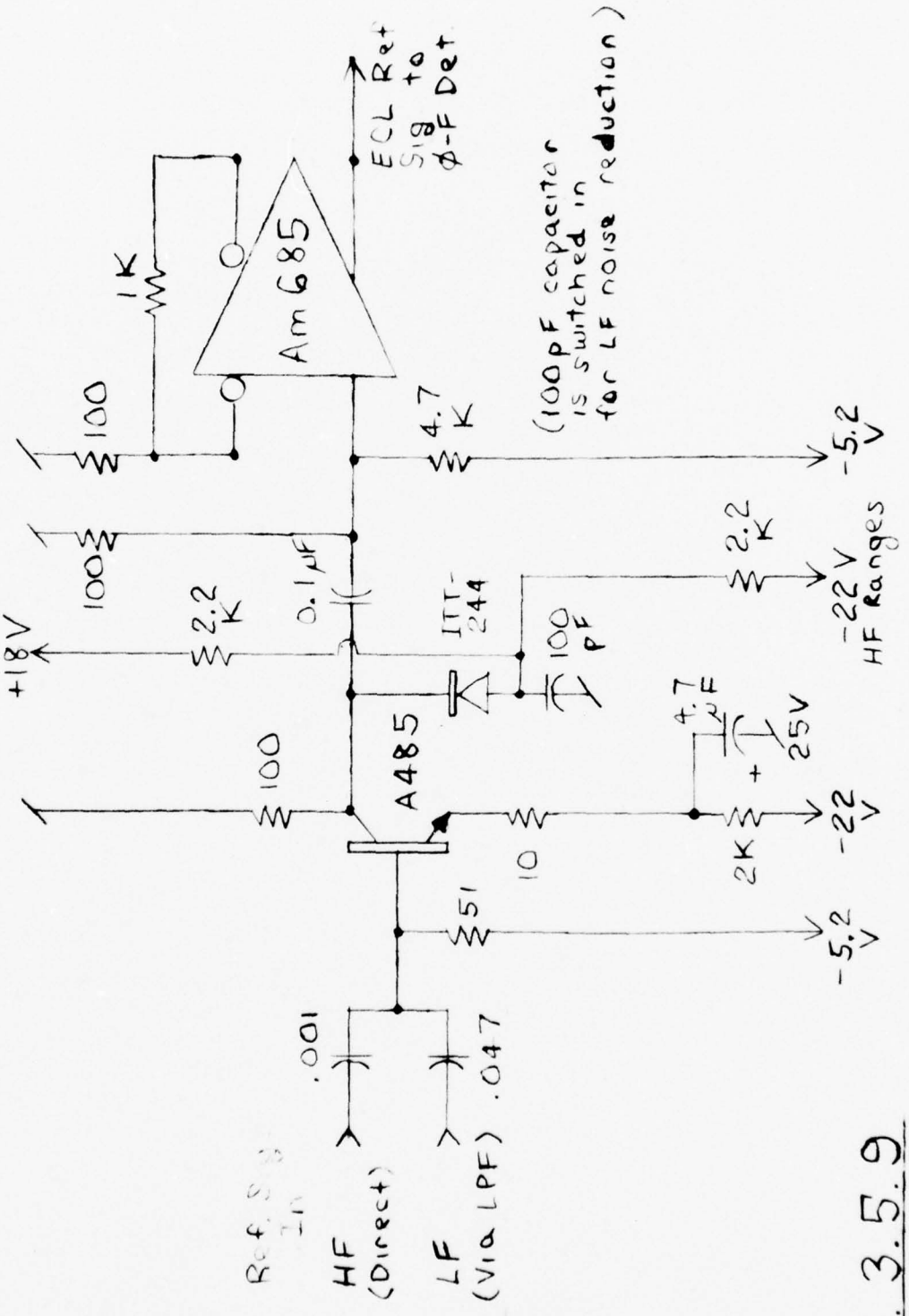


Fig. 3.5.9

REFERENCE SIGNAL AMPLIFIER

SSB PROCESSOR

E6835
WJR
5/18/76
Rev. 7/26/76

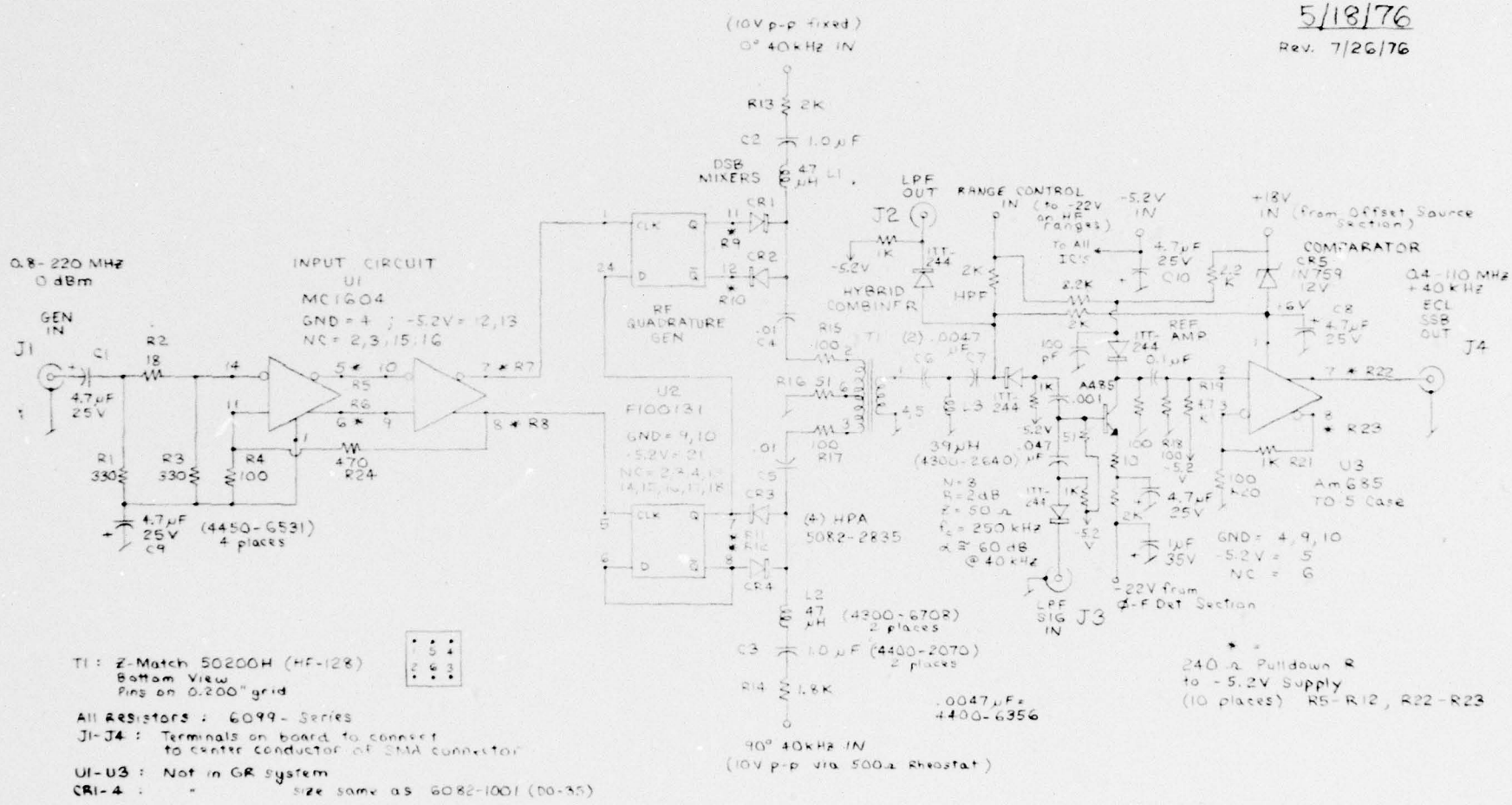


FIGURE 3.5.10 SSB PROCESSOR

3.6 Low Pass Filters

A bank of six low pass filters is necessary to avoid excessive spurious generation in the reference signal comparator. The filters are switched together with the VCO's for the lowest six frequency ranges. No filters are required for the highest six frequency ranges.

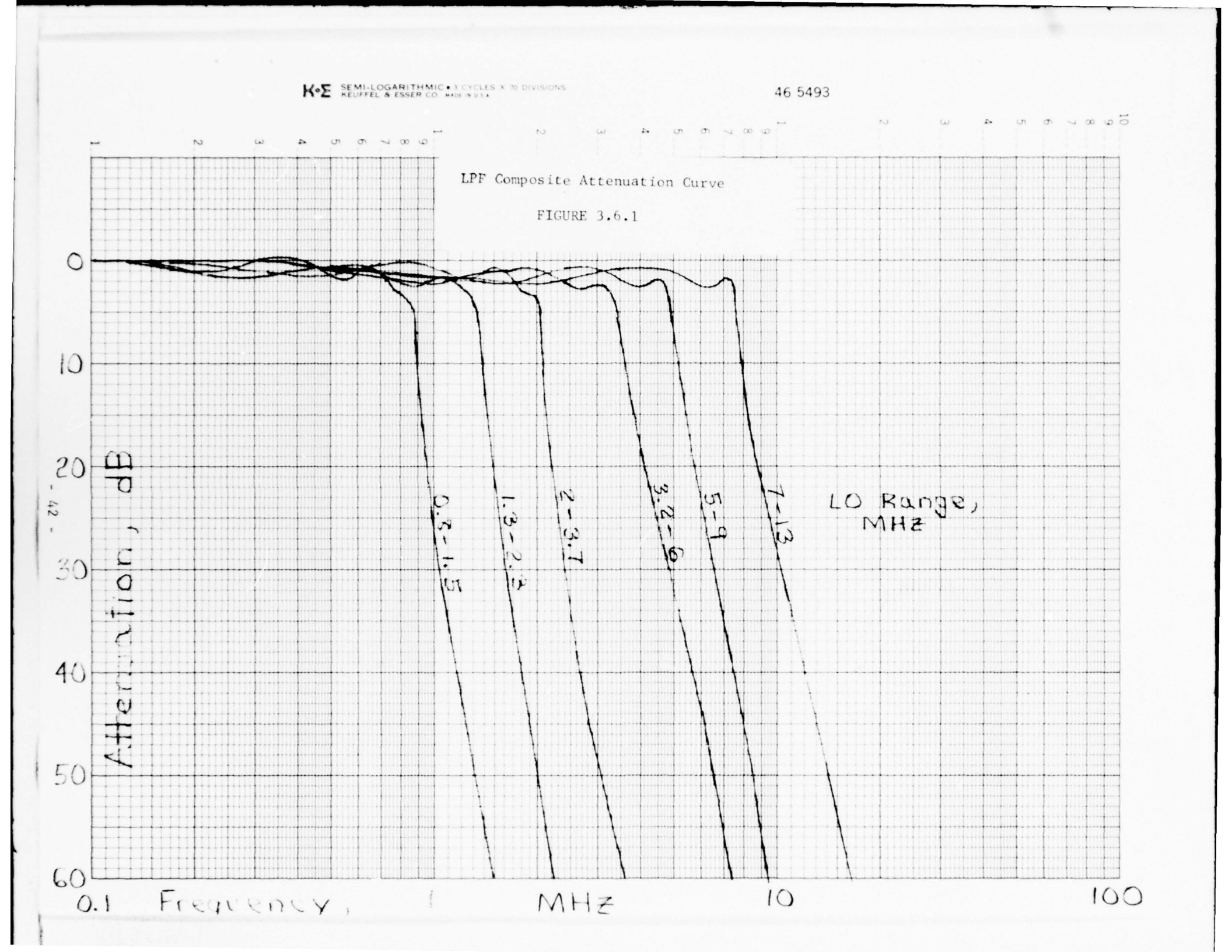
The filters must pass the highest possible reference frequency within each range while attenuating the lowest possible third harmonic component. A sensible choice for cut-off frequency is the lower generator input frequency limit for each range.

Three section filters are used between 0.8 - 3.7 MHz where harmonic attenuation requirements are most severe. Two section filters are used between 3.2 - 13 MHz. All filters are 2 db ripple Chebychev designs at a 50Ω impedance level. The LPF attenuation characteristics are shown in Figure 3.6.1

Filter switching is done with inexpensive PIN diodes. The number of expensive feedthru capacitors is minimized by encoding the range data on four lines (which also carry dc power into the module). A diode matrix encodes the range data outside the module while a standard TTL decoder/driver is used inside. The encoding of range information was decided upon at a time when nine low pass filters were used. Three filters have now been proven unnecessary and direct range switching will be reconsidered for the next design iteration.

The basic filter switching arrangement is shown in Figure 3.6.2. The SSB reference signal from the high pass filter can be routed inside the SSB Processor section directly to the reference signal amplifier or to the LPF module and through one of the low pass filters before returning to the amplifier. The circuit provides reverse bias on the "off" PIN diodes and a forward current of about 5 mA through the "on" diodes.

A complete schematic of the Low Pass Filter Section is shown in Figure 3.6.3.


K•Σ SEMI-LOGARITHMIC • 3 CYCLES X 70 DIVISIONS
KEUFFEL & ESSER CO. MADE IN U.S.A.
46 5493
LPF Composite Attenuation Curve
FIGURE 3.6.1
0
10
20
30
40
50
60
Attenuation, dB
0.3-1.5
1.3-2.2
2-3.7
3.2-6
5-9
7-13
LO Range, MHz
0.1
Frequency, MHz
1
10
100

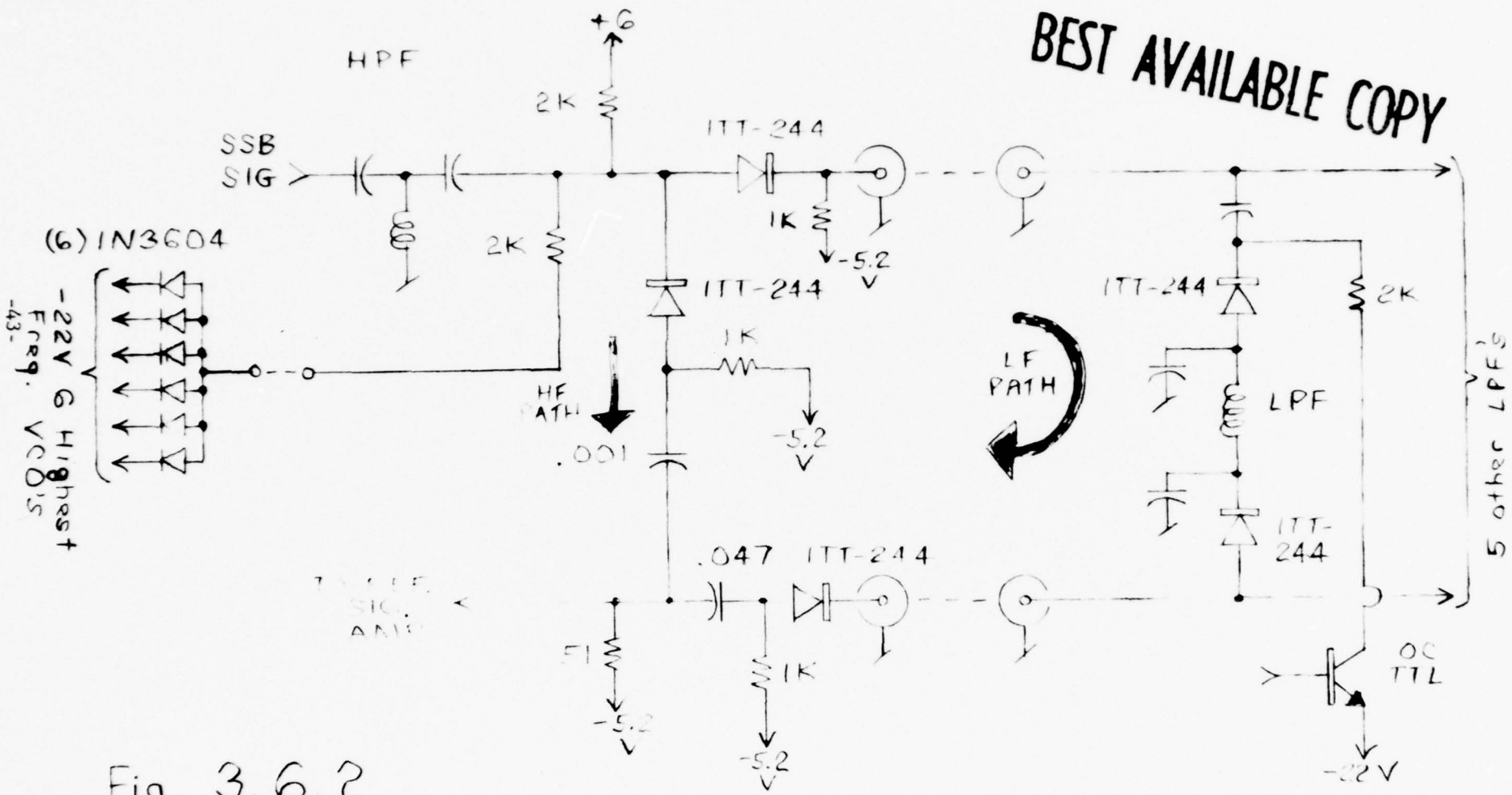


Fig. 3.6.2

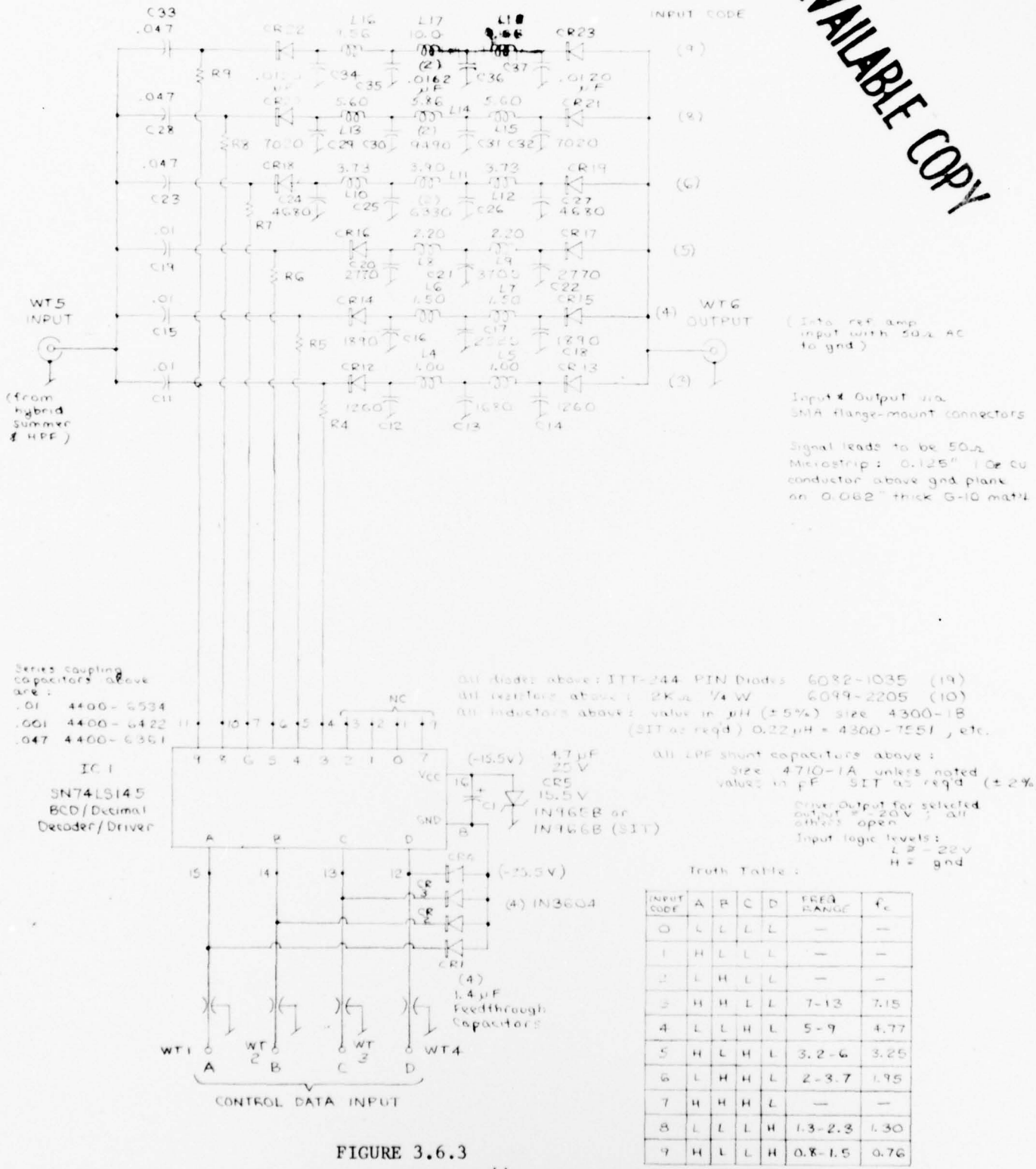
FILTER SWITCHING CIRCUIT

LOW PASS FILTER SECTION

E6835
WJR
4/27/76

Rev. 7/26/76

All filters are Z = 50Ω, R = 2 dB Chebyshev with $f_c \approx$ lower band edge. Exact f_c chosen for 1 inductor nominal std. value.



Truth Table:

INPUT CODE	A	B	C	D	FREQ RANGE	f_c
0	L	L	L	L	—	—
1	H	L	L	L	—	—
2	L	H	L	L	—	—
3	H	H	L	L	7-13	7.15
4	L	L	H	L	5-9	4.77
5	H	L	H	L	3.2-6	3.25
6	L	H	H	L	2-3.7	1.95
7	H	H	H	L	—	—
8	L	L	L	H	1.3-2.3	1.30
9	H	L	L	H	0.8-1.5	0.76

FIGURE 3.6.3

3.7 Phase-Frequency Detector

The primary function of this circuit is to compare the phases of the SSB reference and VCO sample signals, providing an error signal for the phase-lock loop. Secondary functions are to provide loop gain, to detect an unlocked condition and to provide frequency discriminator action to permit lockup. The latter function is very important in a loop of this type where a wide range VCO is to be locked with a narrow loop bandwidth.

The basic phase-frequency detector logic used is shown in Figure 3.7.1. It consists of two set-reset latches (each implemented with two 2-input positive NAND gates) and another gate which is used as a reset generator. The operation of the circuit is as follows:

The first input pulse to arrive sets its corresponding latch. The circuit will remain in this state until a pulse arrives at the other input (whether or not additional pulses arrive at the first input). The pulse at the other input first sets that latch and then the reset gate immediately resets both latches. Thus, the circuit will produce the following outputs:

$f_1 > f_2$ The Q_1 output will be a variable duty ratio pulse train, varying from approximately 0 to 100% at the rate $f = f_1 - f_2$. The Q_2 output will be low except for the duration of the narrow input pulse.

$f_2 > f_1$ The Q_1 and Q_2 outputs will be the reverse of that described above.

$f_1 \approx f_2$ One of the two outputs will be low except for the duration of the narrow input pulse.
The other output will be a certain fixed duty ratio which is dependent on the phase relation of the two input signals.

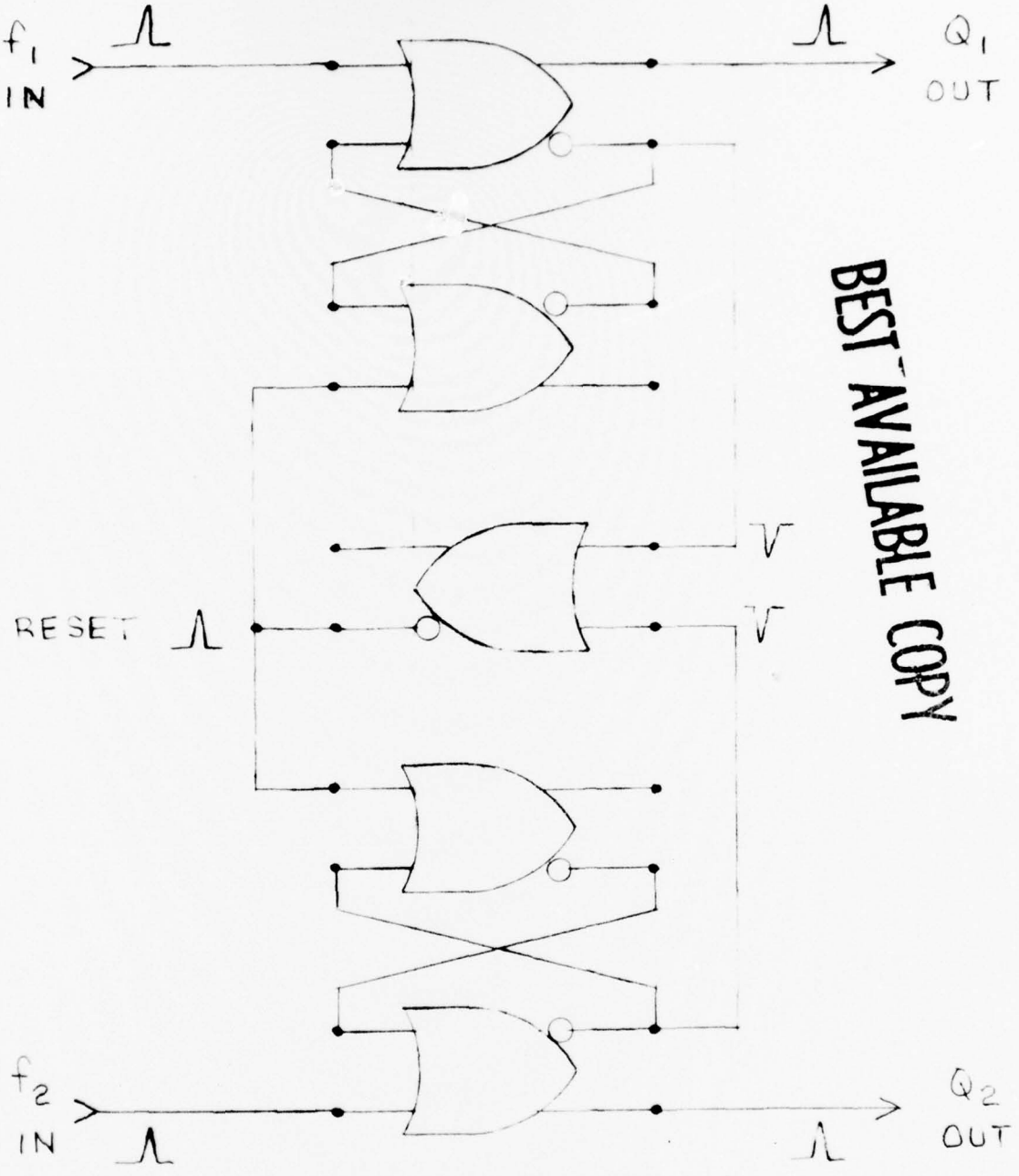


Fig. 3.7.1. Phase - Frequency Detector

3.7 Phase-Frequency Detector (continued)

In use in a phase-lock loop with high dc gain, this phase detector will operate at a nominal 0° phase relation. Both outputs will be low except for identical positive pulses during the duration of the (coincident) input pulses. The output, which is taken differentially, is the nearly-zero signal determined by the static error coefficient set by the dc loop gain. Since both outputs are identical it becomes immaterial from which direction the loop approached lock. But before lock, when $f_1 \neq f_2$, an error signal is produced which forces the loop toward the condition $f_1 = f_2$ and $\phi_1 = \phi_2$.

Various implementations of this basic Ø-F detector logic are available in integrated circuit form, but none has sufficient frequency range (110 MHz) for this application. It was found necessary to use subnanosecond ECL devices to insure proper operation. A Fairchild F100102 quint 2-input gate used in the configuration of Figure 3.7.1 has considerable margin above 110 MHz.

This Ø-F detector requires that the inputs be short positive pulses which are generated by the arrangement shown in Figure 3.7.2. The output pulse duration is determined by the propagation delay of the first gate plus the RC time constant.

The phase-frequency detector produces coincident output pulses only under locked conditions. This is the operating principle of the unlock-alarm circuit shown in Figure 3.7.3.

The coincidence of the detector pulses is sensed by the exclusive-nor logic function which has an output that is high when the loop is locked and a variable duty ratio pulse train when the loop is unlocked. The resulting change in dc voltage is detected by a comparator which drives the unlock-alarm light. The unlock alarm will warn of any of the following conditions:

1. No reference signal.
2. No oscillator signal.
3. Reference signal outside lock range of oscillator.

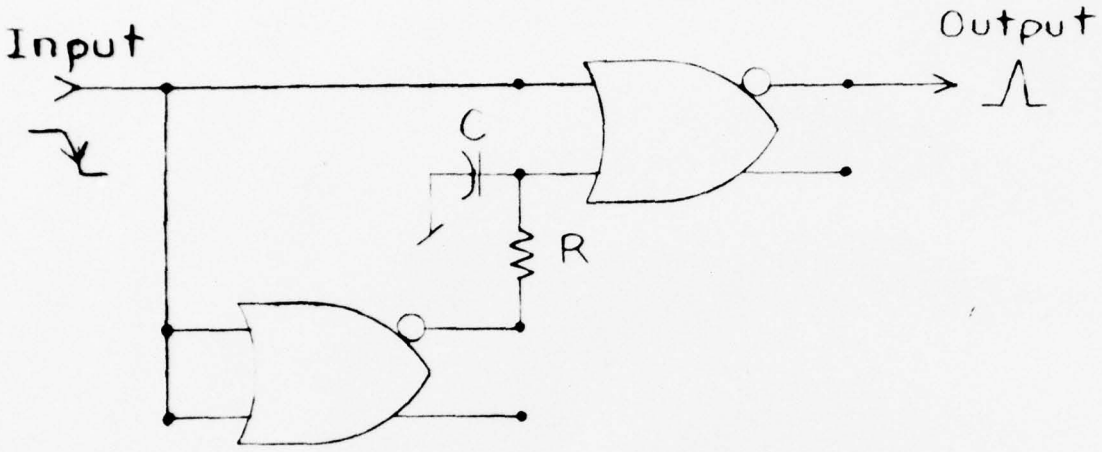


Fig. 3.7.2. Pulse Generator

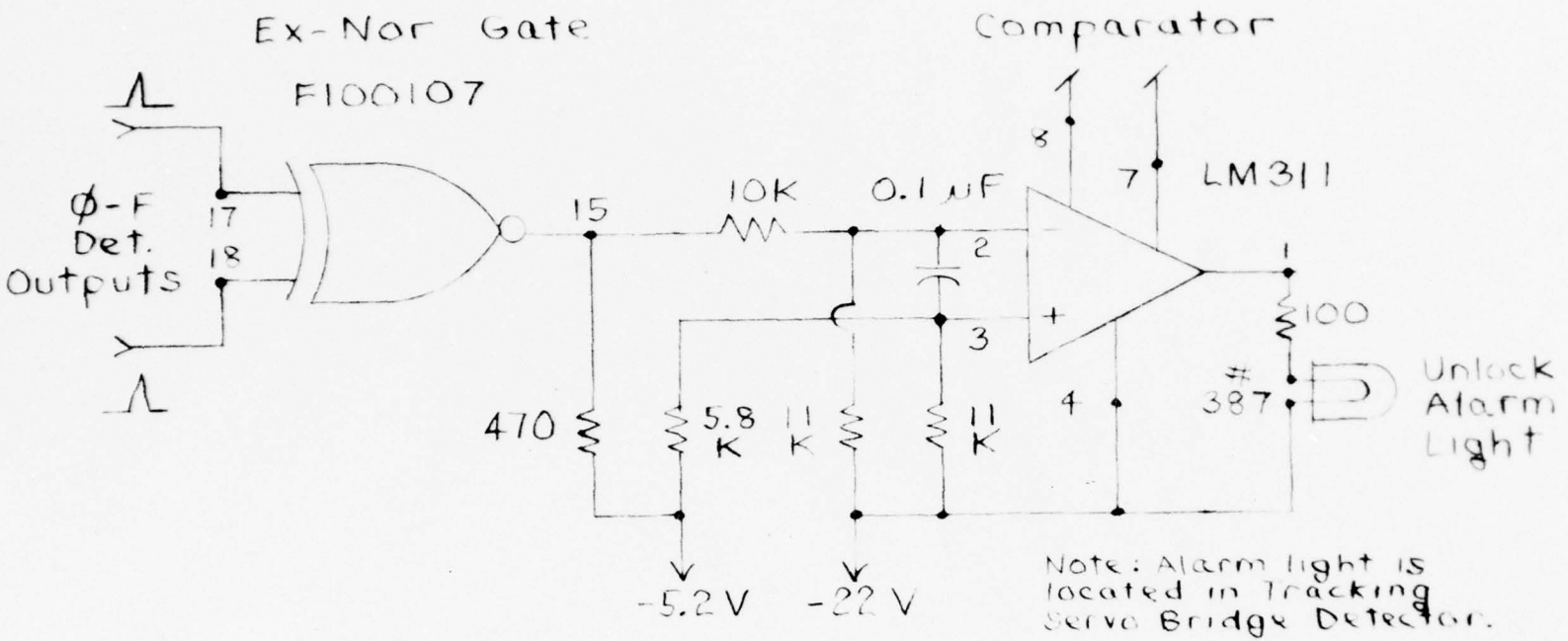


Fig. 3.7.3. Unlock Detector

3.7 Phase-Frequency Detector (continued)

4. AC on lock loop for any reason.
5. Failure of the VCO, Output Amplifier, Isolation Amplifier, Offset Source, SSB Processor or Loop Amplifier.
6. Loss of -5.2, -18 or +18V supplies.
7. Most failures of Phase-Frequency Detector.

Loss of the -22V supply, while not indicated by the alarm, will result in no LO output, thus no wrong output. The alarm circuit itself can be checked by simply switching to an improper frequency range and observing that the alarm light comes on.

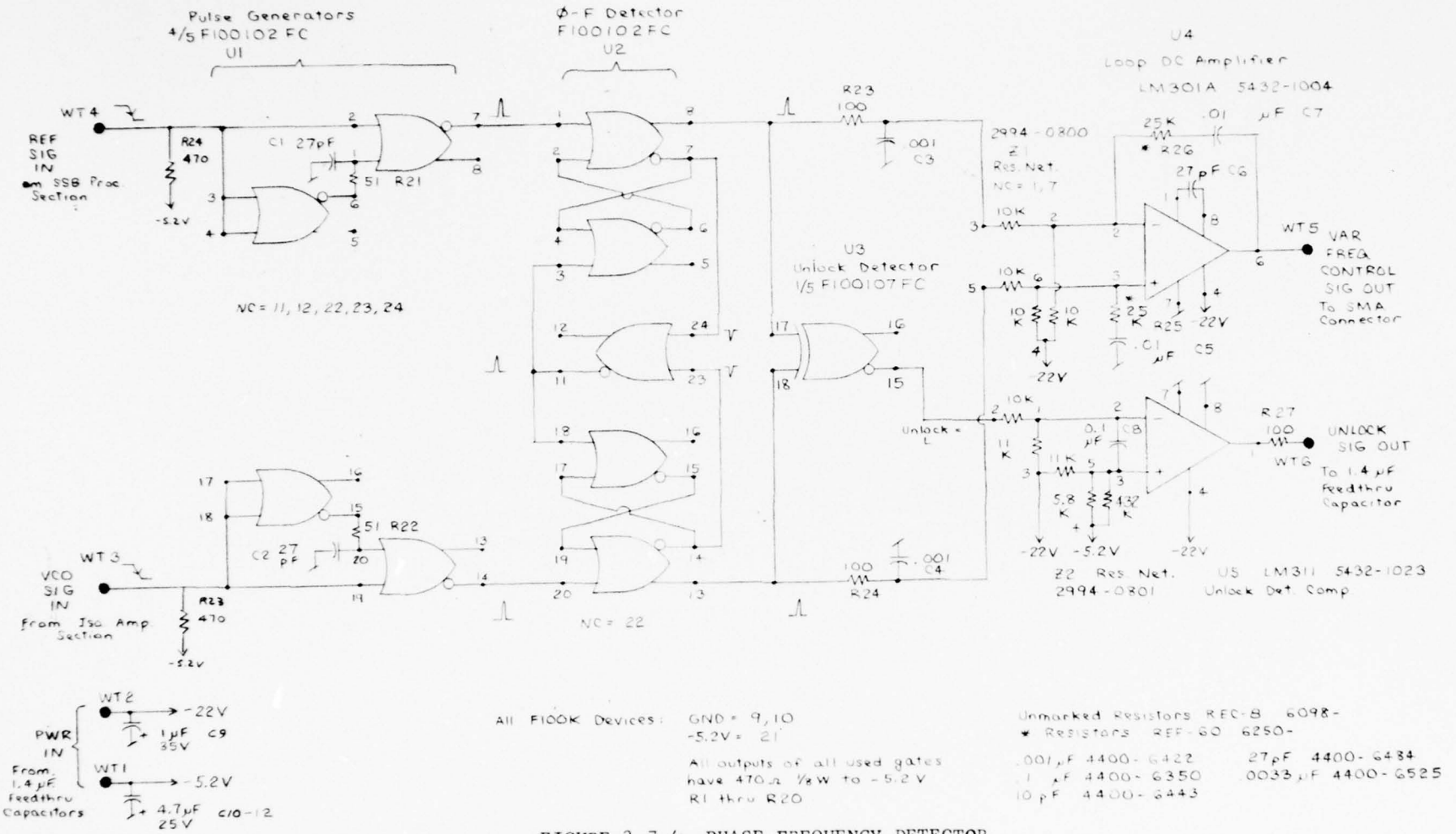
The error voltage for the phase lock loop is produced by an operational amplifier which accepts the differential signals from the Ø-F Detector. This amplifier has several passive networks associated with it that provide pulse filtering, dc translation and ac gain shaping. A detailed discussion of the lock loop design is given in the next report section.

An important factor in the application of this type of digital Phase-Frequency detector is its sensitivity to phase discontinuities of the input signals. The circuit is tolerant of continuous phase jitter on the input signals, with a deviation of up to a considerable fraction of a carrier period, but will interpret a sudden phase "glitch" as a frequency error which will drive the detector against the stop. Loop filtration will not materially smooth such a disturbance of the broadband Phase-Frequency detector itself. It is especially important in this application to avoid any quasi-coherent pulsed noise pickup which can drift through the reference comparator threshold, causing a sudden phase discontinuity which can seriously perturb the lock loop.

The schematic diagram of the complete Ø-F Detector circuit is shown in Figure 3.7.4.

Ø-F DETECTOR SECTION
using F100K Ø-F DET LOGIC

E6835 10/14/75 WJR
REV. 10-29-75 BLD
7/26/76 WJR



All F100K Devices: GND = 9, 10
-5.2V = 21
All outputs of all used gates have 470Ω 1/8W to -5.2V
R1 thru R20

Unmarked Resistors REC-B 6098-
* Resistors REF-60 6250-

.001 µF 4400-6422
.1 µF 4400-6350
10 pF 4400-6443
27 pF 4400-6484
0033 µF 4400-6525

FIGURE 3.7.4 PHASE-FREQUENCY DETECTOR

3.8 Loop Filter

The frequency response of the VCO lock loop must be rather carefully shaped to produce a satisfactory LO signal output. The loop bandwidth must be wide enough to insure a low noise level near the carrier and to provide adequate response speed for lock up and sweeping. But the loop must also serve as an effective filter for spurious sidebands at 40 and 80 kHz. Furthermore, the LO spectrum should be free from pronounced "bumping up" of noise sidebands at the loop natural frequency. These constraints require careful control of the phase and magnitude of the open-loop gain.

An analysis of the lock loop is shown in Figure 3.8.1. The loop elements are:

(1) The ECL Ø-F Detector with a transfer function $K_{\emptyset}$ = 0.2 volts/radian.
(2) The Main Loop Amplifier with a midband transfer function K_a = 2.5 volts/volt.
(3) The Cauer Loop Filter with a null at 40 kHz.
(4) The Varactor Linearizing Amplifier and Voltage Limiting Network.
(5) The Lead-Lag Compensation Network associated with each VCO.

The main objective in the loop design is to obtain both a steep increase in gain below the unity gain frequency and a steep decrease in gain above the unity gain frequency while insuring a stable servosystem. A nominal 5 kHz unity gain frequency is chosen as a compromise between the 2 kHz detector IF bandwidth (where loop gain is desired) and the 40 kHz offset frequency (where loop attenuation is desired). The Main Loop Amplifier and VCO Compensation Network each have downbreaks at 1 kHz which contribute around 10° phase lag at 5 kHz. The VCO varactor feed circuits have 30 kHz downbreaks which also contribute around 10° phase lag at 5 kHz.

PLL ANALYSIS

E6835
WJR
9/23/75
Rev 1/26/76
7/26/76

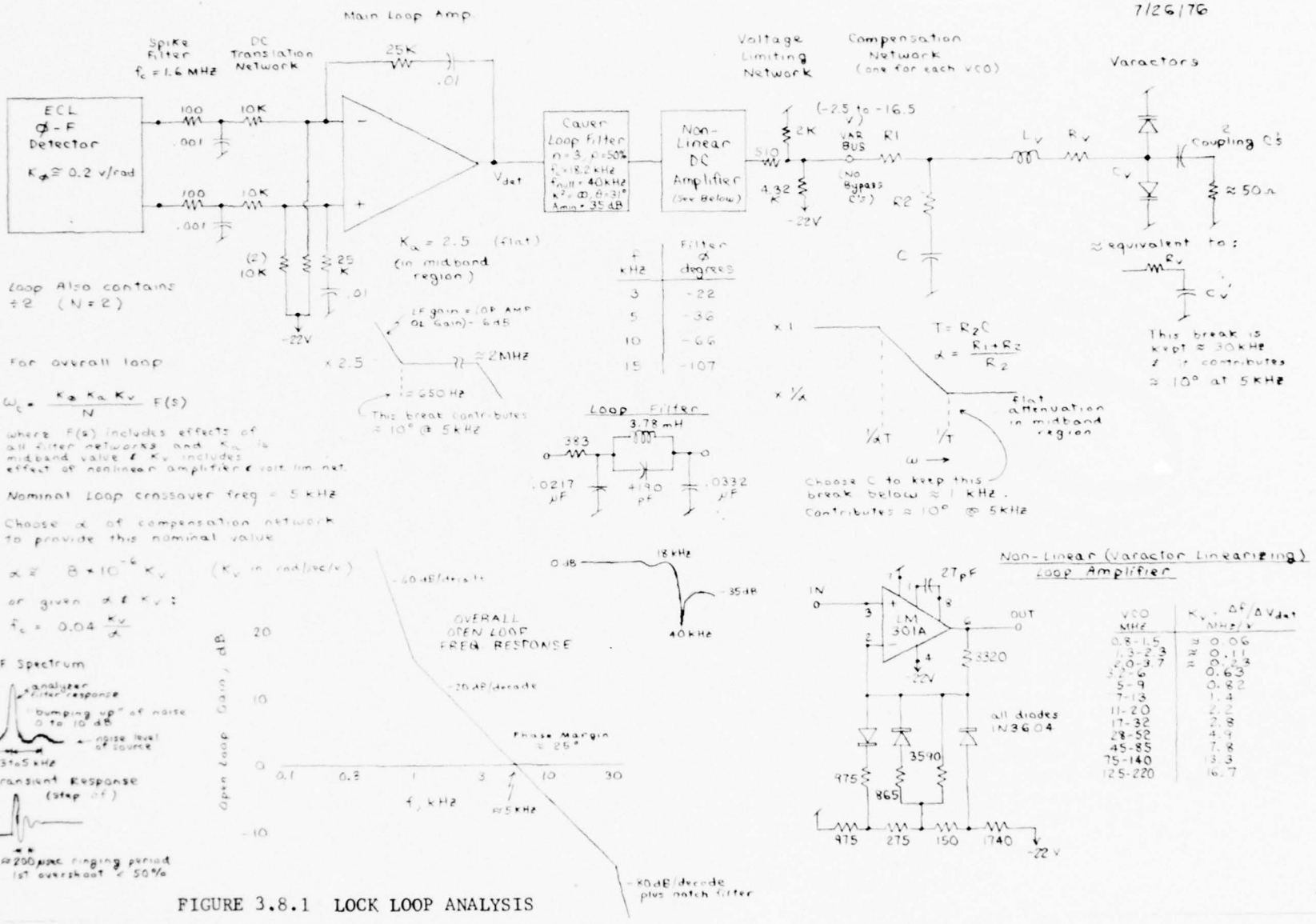


FIGURE 3.8.1 LOCK LOOP ANALYSIS

3.8 Loop Filter (continued)

The intrinsic VCO integration contributes 90° phase lag, bringing the total to 120°. If a phase margin of 25° is desired for the overall system, the Loop Filter may contribute 35° at 5 kHz.

A Cauer (Elliptic) Low Pass Filter was chosen as best suited for this application. The design has a 18.2 kHz cut-off frequency, a null at 40 kHz and a minimum stop band attenuation of 35 dB.

Such careful loop shaping would be futile if applied directly to a varactor tuned VCO which exhibits the typical 5:1 tuning slope variation over the control voltage range. These variations are reduced by restricting the applied voltage to avoid unnecessary overrange and by a non-linear dc amplifier which provides a 4-segment approximation to compensate for the varactor characteristic. The varactor characteristics are shown in Figure 3.8.2, and the linearizing amplifier in Figure 3.8.3. These circuits are packaged on the Loop Filter Module shown in Figure 3.8.4.

Extensive tests were made on the dynamic behavior of the lock loop for each of the twelve VCO's. The loop can become unstable for either high or low gain conditions as evidenced by excessive ringing of the control voltage to step changes in frequency and by a "bumping up" of the noise sidebands on either side of the output frequency. The low gain condition is particularly undesirable because it results in a low natural frequency of the loop, longer transient settling time, poor VCO noise reduction and pronounced "bumping up" of noise sidebands close to the carrier. The series resistor (R1) of the VCO Compensation Network was adjusted during these tests (during which a direct lock was made to the reference input without offset) for each VCO.

Typical results obtained in these tests are shown in Figure 3.8.5. The 4.0 and 5.0 MHz transient response and spectra represent the extreme conditions of a high (4.0 MHz) and low (5.0 MHz) gain loop. A comparison between the spectra shows slight noise bumping at ±4 kHz vs more pronounced noise bumping at ±2 kHz. A comparison between the transient responses shows a relatively fast, ringing response vs one that is slower and more sluggish.

Varactor Characteristic

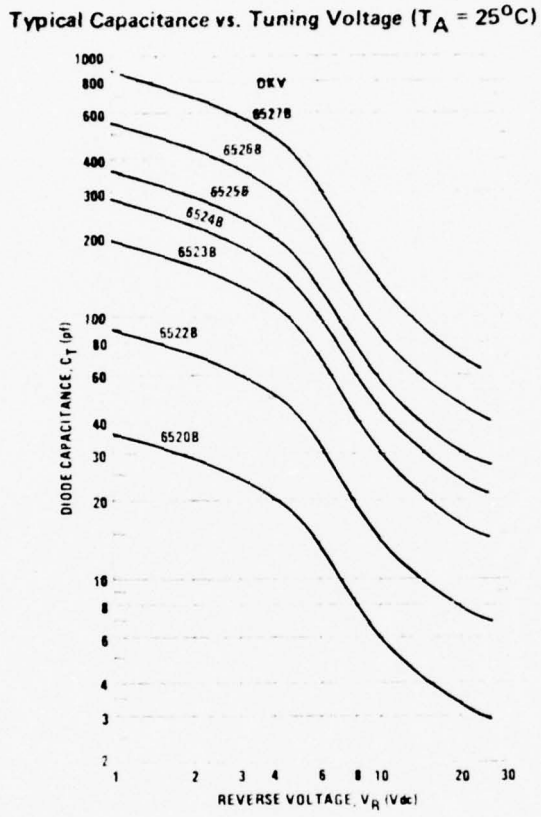
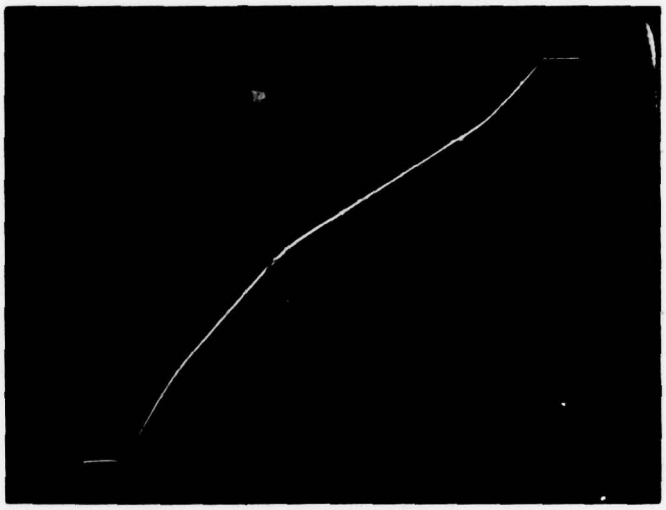


FIGURE 3.8.2

Varactor Linearizing Amplifier

Transfer Characteristic



Horizontal Scale: V_{in} 1 volt/div
-8.5 volt center

Vertical Scale: V_{out} 2 volts/div
-9.5 volt center

FIGURE 3.8.3

LOOP FILTER SECTION

E-6835 WJR

2/5/76

Rev. 2/9/76
7/26/76

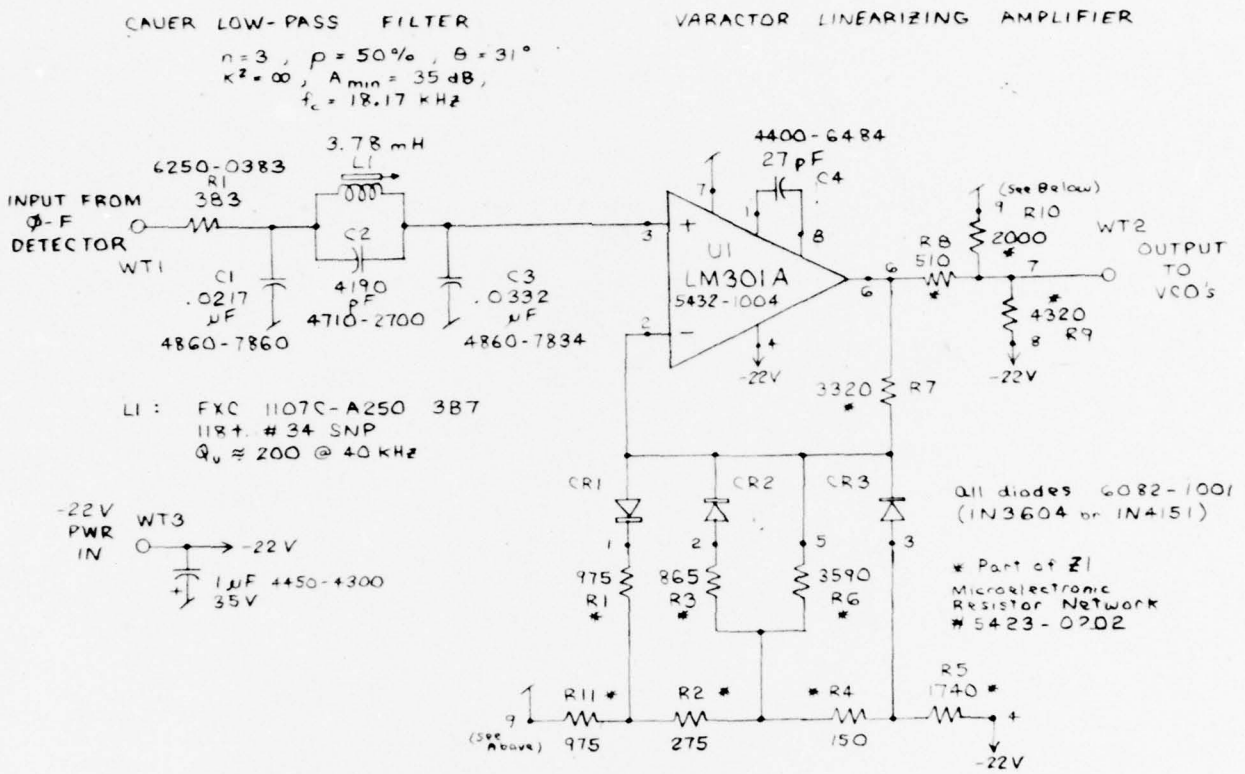
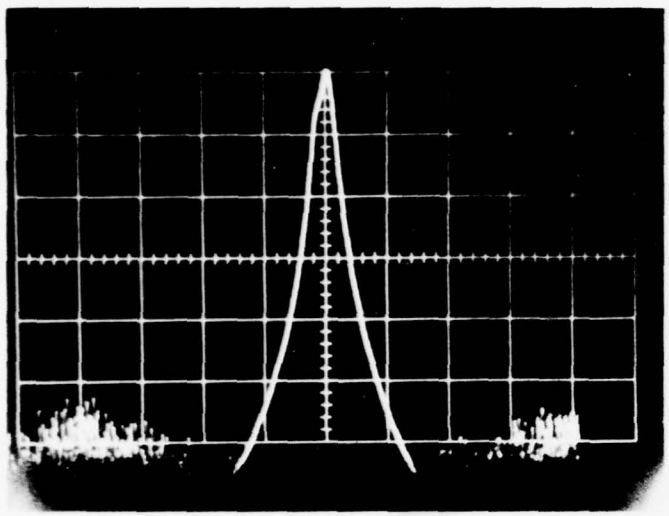
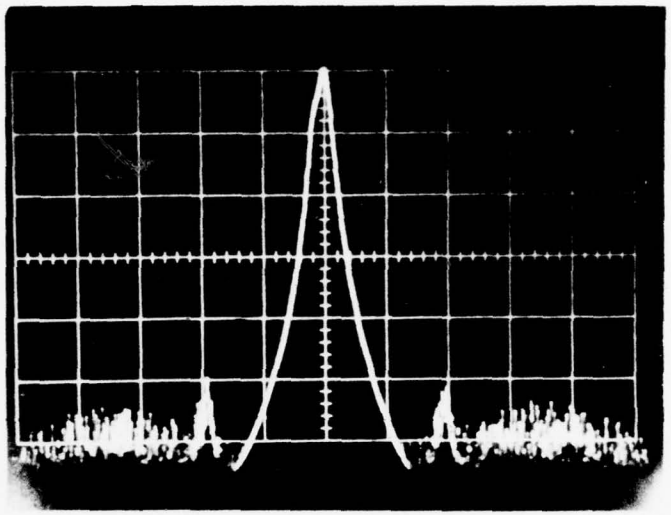


FIGURE 3.8.4 LOOP FILTER

FIGURE 3.8.5

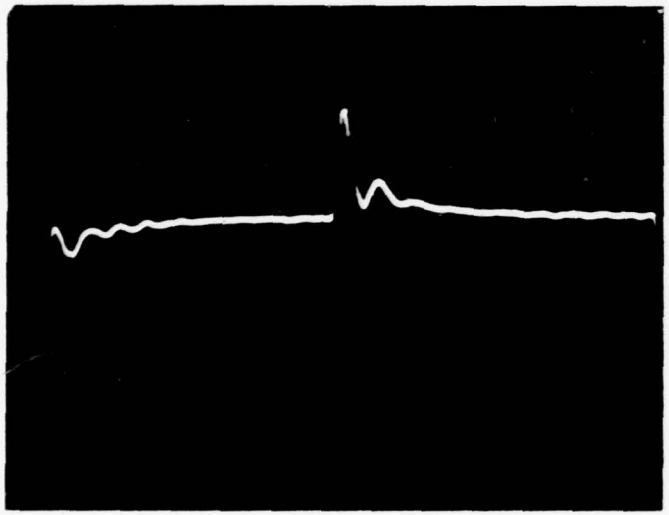
EXTREMES FOR LOOP RESPONSE



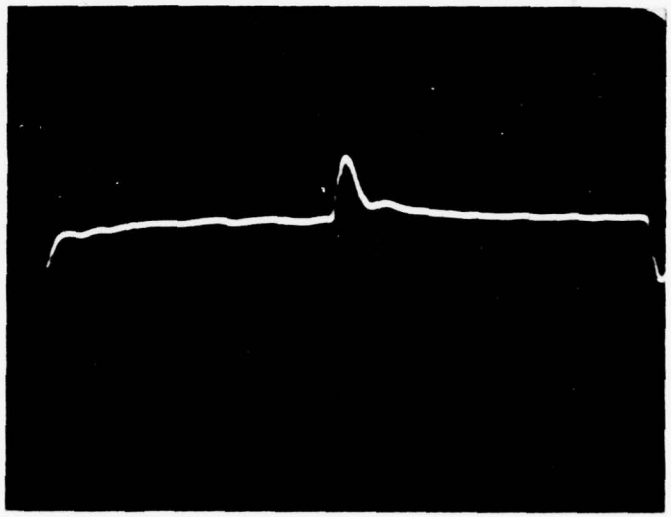


LO SPECTRUM

1 kHz/div. horiz.
10 dB/div. vert.
RF & Video BW 100 Hz



4.0 MHz



5.0 MHz

LOOP TRANSIENT RESPONSE

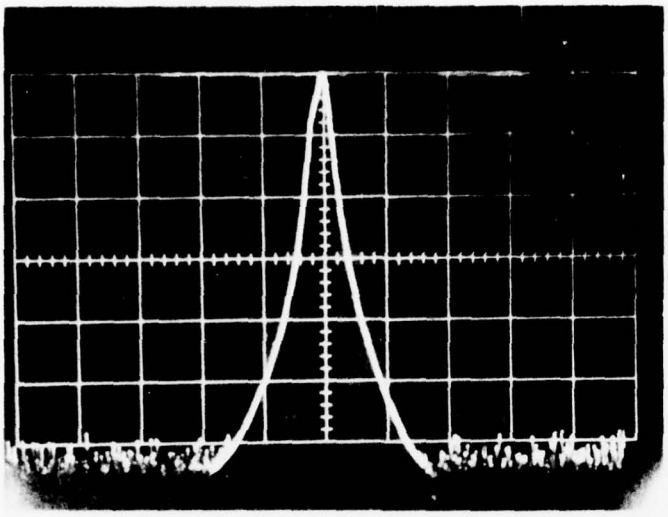
500 µsec/div. horiz.
200 mV/div. vert.

3.8 Loop Filter (continued)

Figures 3.8.6 through 3.8.9 show typical results over the entire frequency range. It is believed that the loop design achieves near-optimum performance for this application.

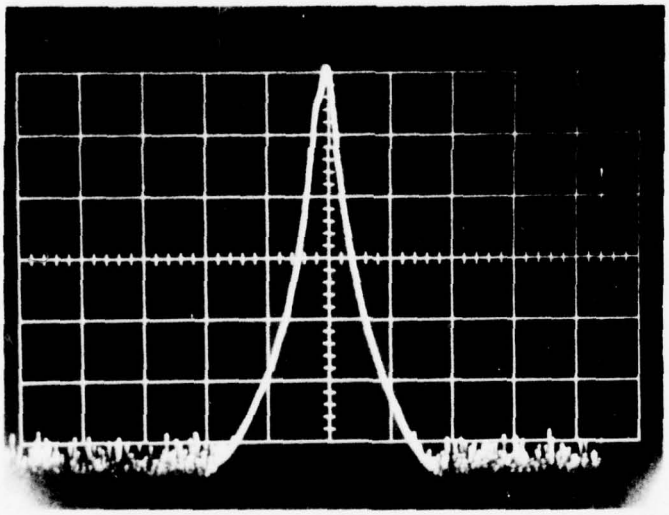
0.8 MHz (0.8-1.5 MHz VCO) LOOP RESPONSE

FIGURE 3.8.6



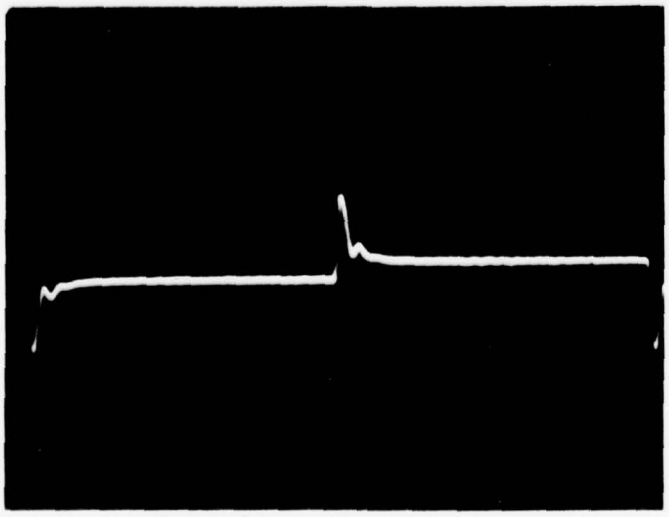
LO OUTPUT SPECTRUM

1 kHz/div. horiz.
10 dB/div vert.
RF BW 100 BW 100 HZ



GEN INPUT SPECTRUM

(Same scale factors as above)

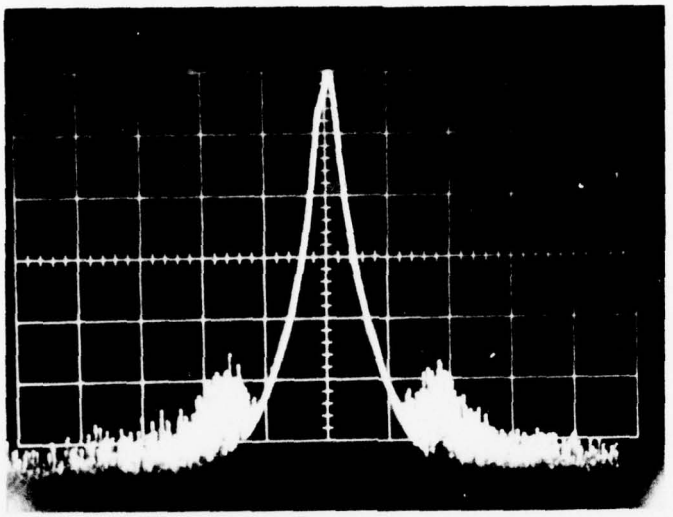


LOCK LOOP TRANSIENT RESPONSE

500 µsec/div horiz.
100 mV/div vert.

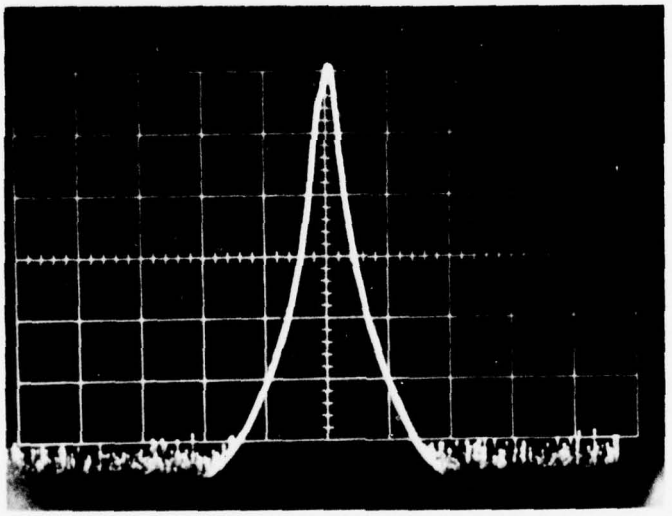
10 MHz (11-20 MHz VCO) LOOP RESPONSE

FIGURE 3.8.7



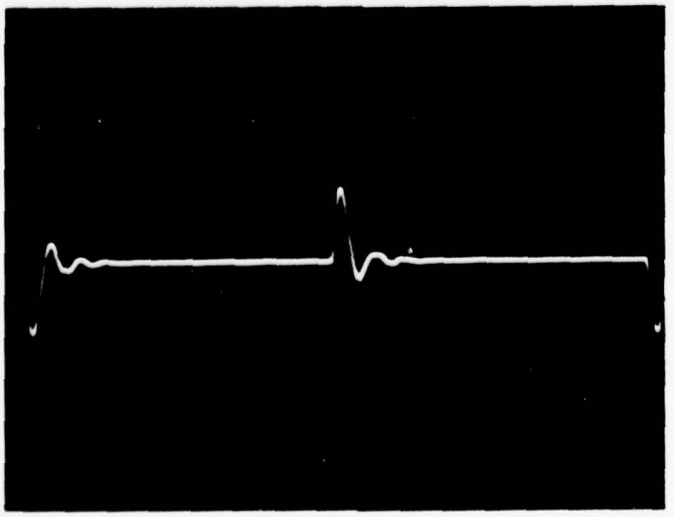
LO OUTPUT SPECTRUM

1 KHz/div horiz.
10 dB/div. vert.
RF BW 100 Hz
Video BW 100 Hz



GEN INPUT SPECTRUM

(Same scale factors as above)

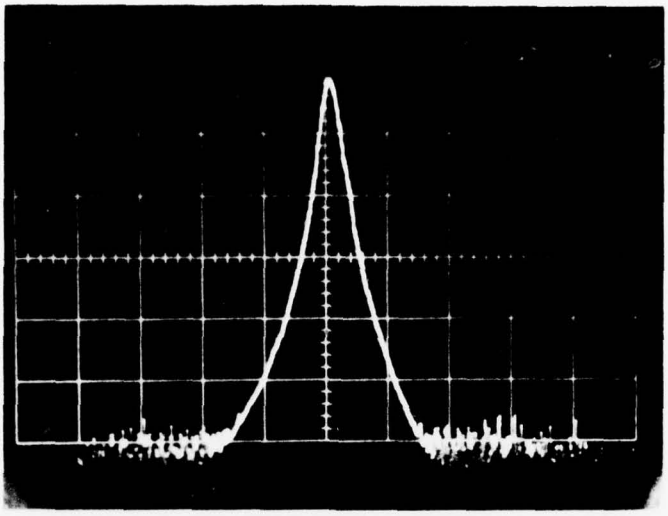


LOCK LOOP TRANSIENT RESPONSE

500 µsec/div. horiz.
200 mV/div. vert.

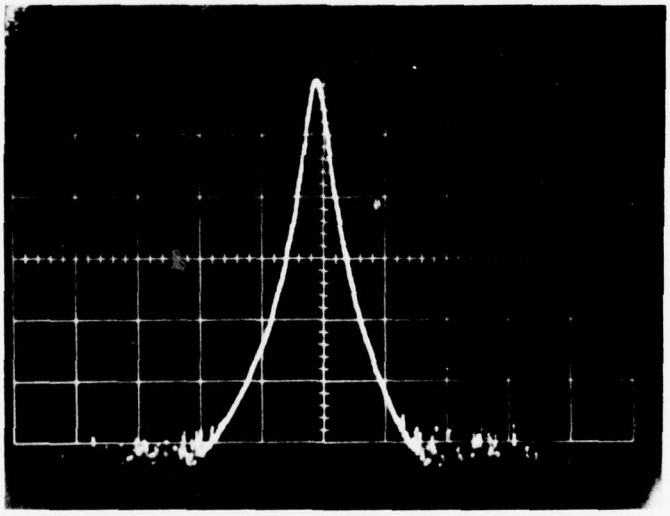
50 MHz (45-85 MHz VCO) LOOP RESPONSE

FIGURE 3.8.8



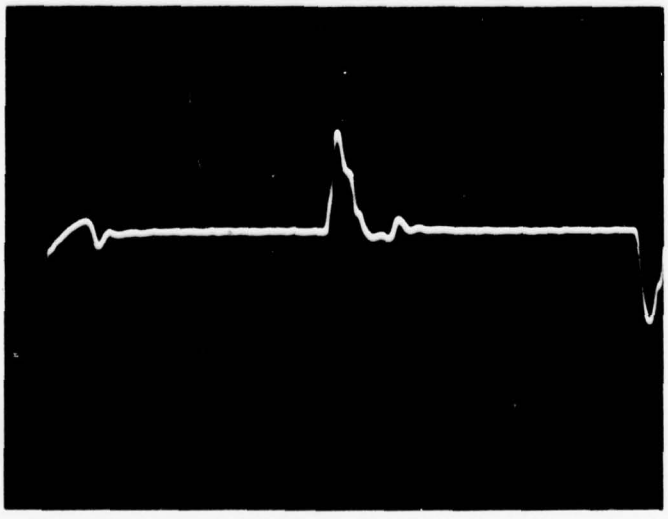
LO OUTPUT SPECTRUM

2 KHz/div horiz.
10 dB/div. vert.
RF BW 300 Hz
Video BW 100 Hz



GEN INPUT SPECTRUM

(Same scale factors as above)

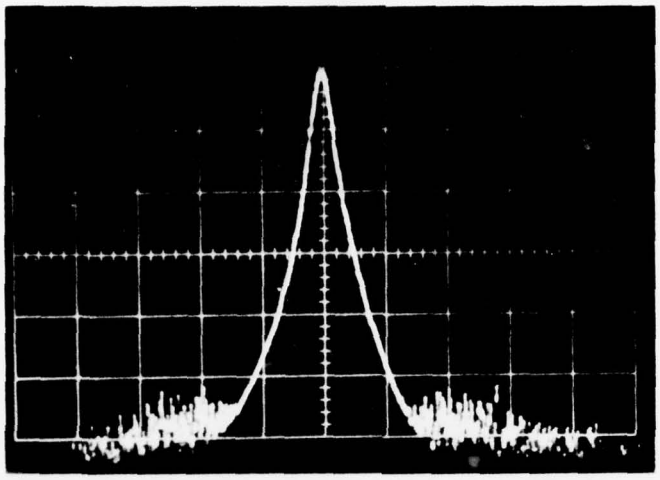


LOCK LOOP TRANSIENT RESPONSE

500 µsec/div horiz.
100 mV/div vert.

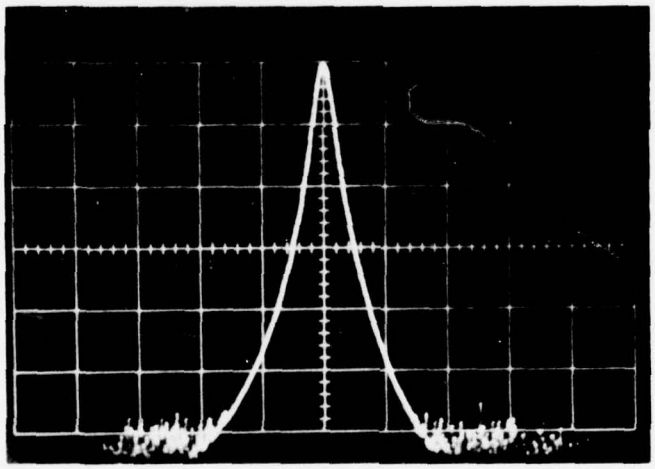
220 MHz (125-220 MHz VCO) LOOP RESPONSE

FIGURE 3.8.9



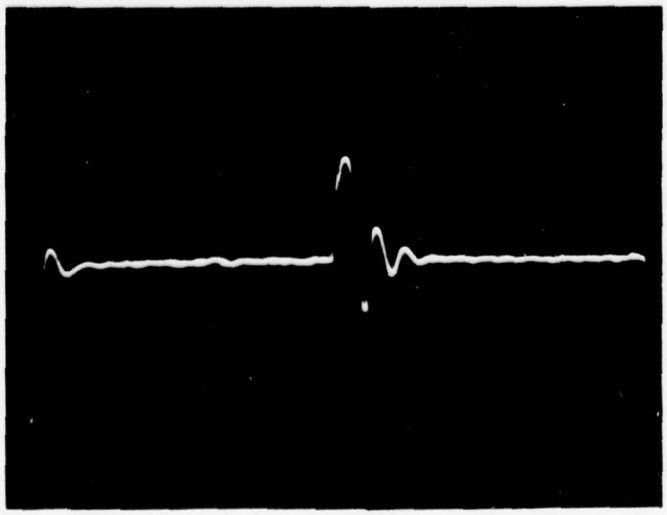
LO OUTPUT SPECTRUM

2 kHz/div horiz.
10 dB.div. vert.
RF BW 300 Hz
Video BW 100 Hz



GEN INPUT SPECTRUM

(Same scale factors as above)



LOCK LOOP TRANSIENT RESPONSE

500 µsec/div horiz.
200 mV/div vert.

4. MECHANICAL PACKAGING

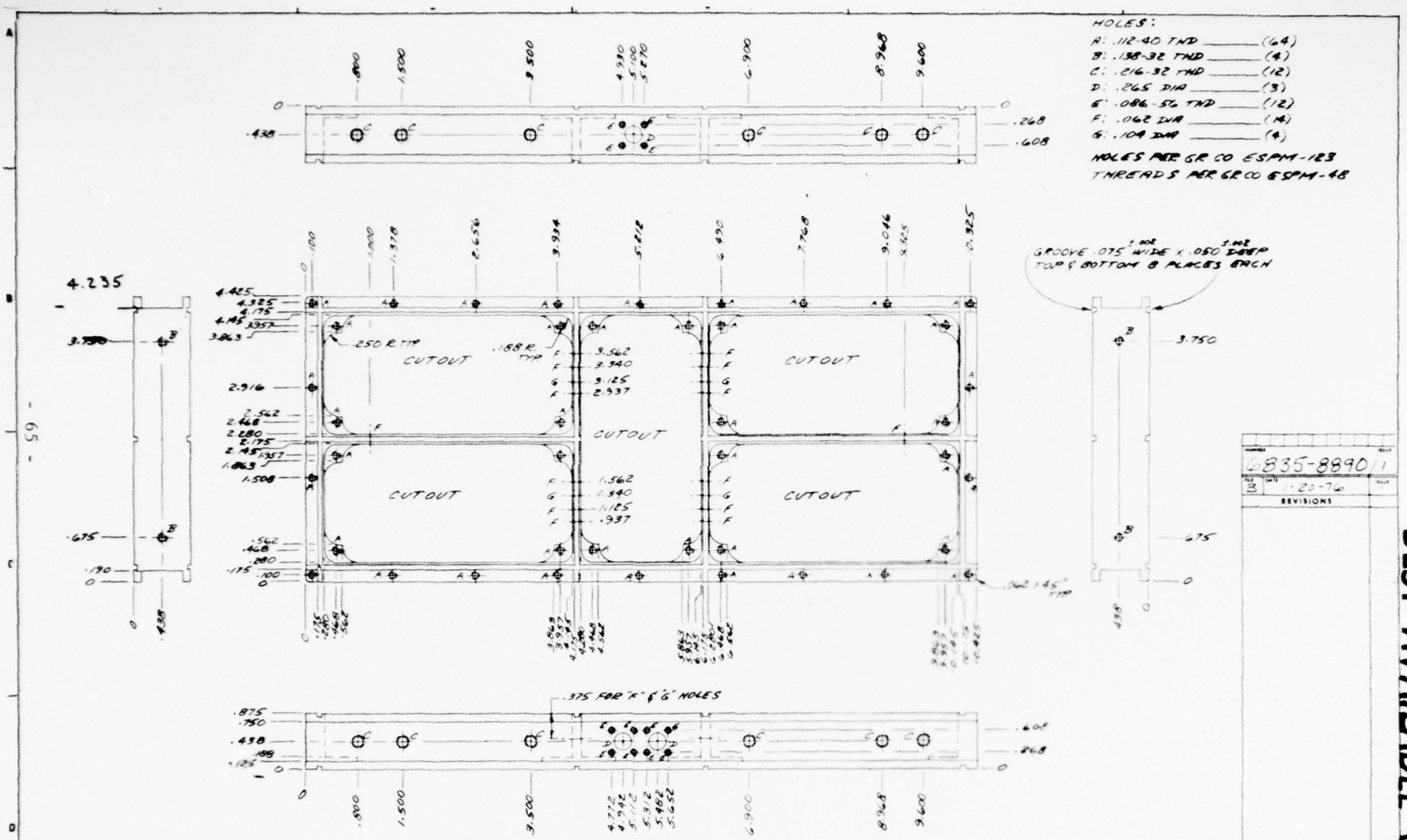
The most important packaging consideration for the Offset LO is a circuit housing which provides extremely effective electrical shielding. A solid housing with RFI gasketing, high performance feedthru filters for all power leads and SMA connectors with solid jacketed coaxial cable for all signal leads was proven mandatory during the preliminary design study which preceded this work.

The Offset LO consists of three modules. The VCO and Lock-Loop Modules each contain five sections (3.8" x 1.8" etched circuit boards) and are identical except for power and signal leads. The smaller Low Pass Filter Module contains a single section. All module housings are machined from solid brass stock and silver plated. Top and bottom covers of the same material compress RFI gaskets set in grooves which shield each section separately. The module housings are shown in Figures 4.1 through 4.3.

The overall mechanical design consists of a skeleton frame which supports the three module housings in a 1-3/4" high unit with a blank front panel and depth compatible with the Tracking Servo Bridge Detector. The unit weighs 23 pounds including the outer cover.

The Offset LO is designed to meet all environmental conditions specified for the Tracking Servo Bridge Detector. Vibration tests were made during mechanical design to verify the strength and rigidity of the package. All metal surfaces have a corrosion resistant finish.

Input and output signals are brought to SMA connectors on the rear panel, which also holds a 24 pin Amphenol connector for power and control leads.



SHIELDING ENCLOSURE

MAT'L: BRASS 360 1/2 HARD

FINISH: HIGH CONDUCTIVITY SILVER PLATE PER GR CO ESFP-24

TOLERANCE:
EDGE TO EDGE ±.015
EDGE TO HOLE ±.015
HOLE TO HOLE ±.005

FIGURE 4.1 VCO MODULE HOUSING

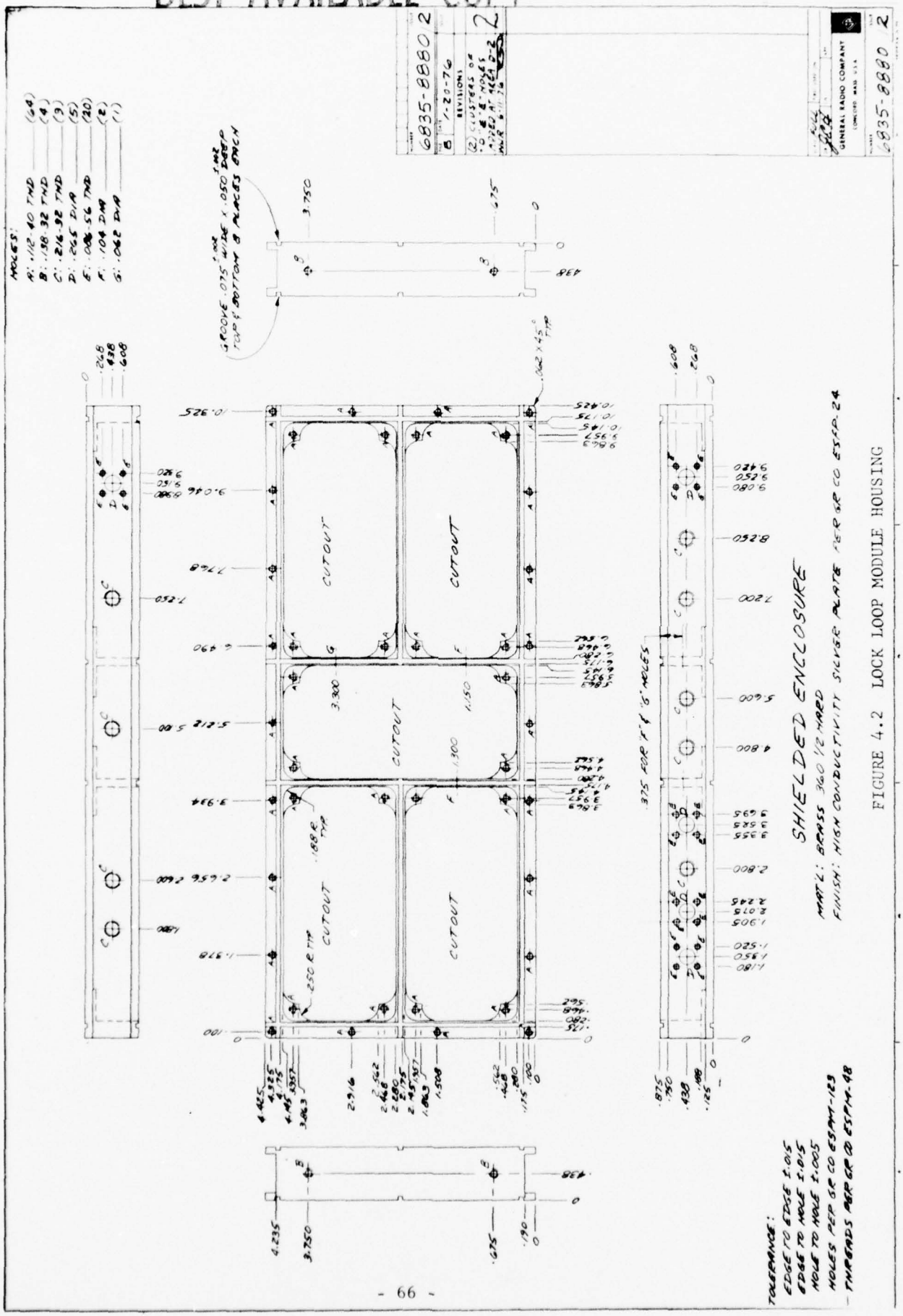


FIGURE 4.2 LOCK LOOP MODULE HOUSING

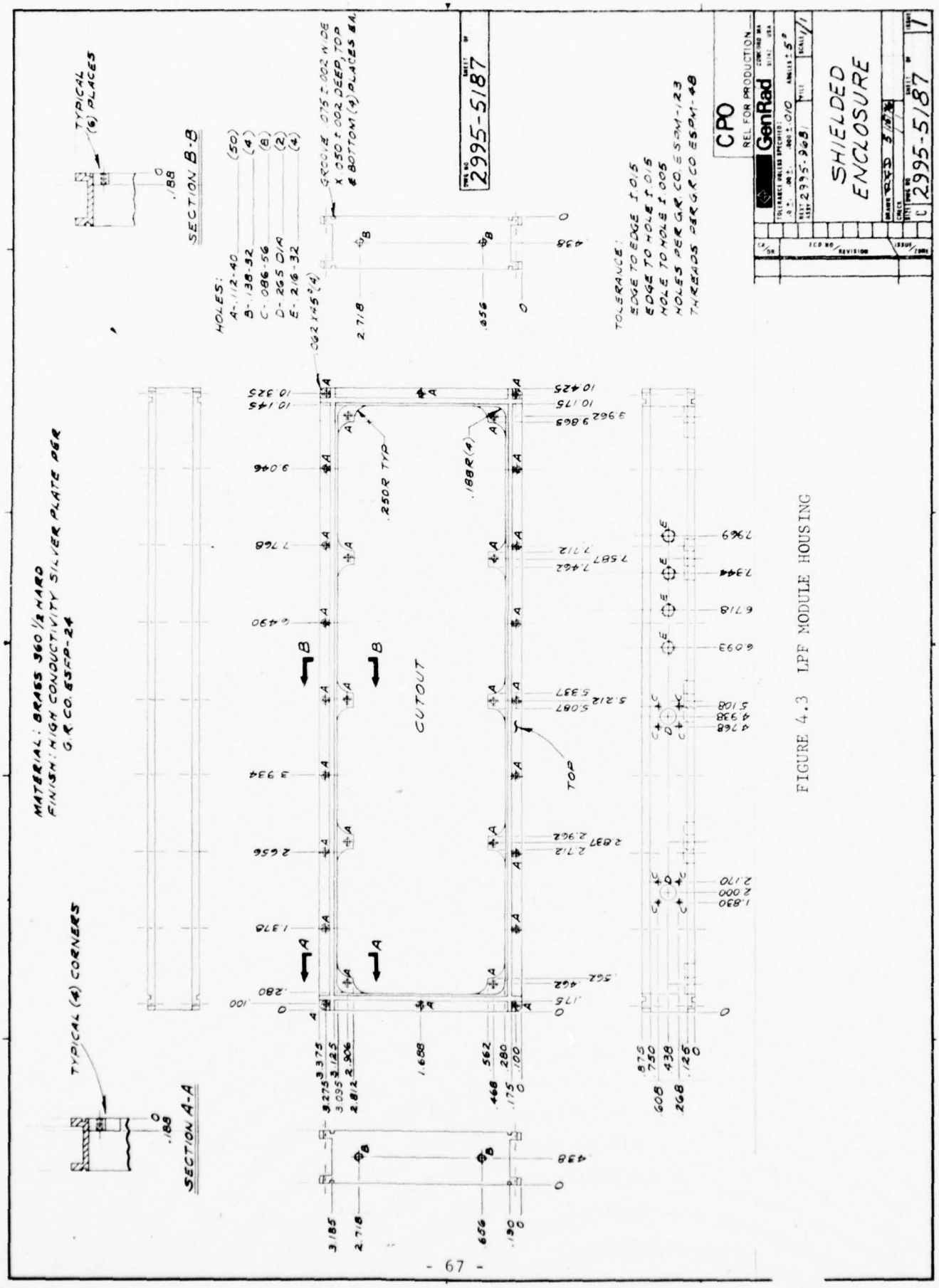


FIGURE 4.3 LPF MODULE HOUSING

5. TEST RESULTS

A total of three Offset LO units have been built and tested. All units have performed satisfactorily and it is believed that a viable design has been achieved. This report section will describe the results of these tests.

The lock ranges for each unit are shown in Figures 5.1 through 5.3. The ranges are deliberately restricted from exceeding the nominal amounts in order to avoid large changes in tuning sensitivity and consequently better loop stability. The nominal ranges are arranged to have considerable overlap and further overlap is of no particular advantage. All units have comfortable lock margins at both frequency extremes. There are a few places where the actual tuning range is not properly centered, but can be corrected simply by adjusting the VCO tank inductor. Adequate overlap was still available, however. The only real question related to the VCO design is a tendency toward "squegging" on some of the LF ranges under certain load conditions. This problem is caused by RF parasitic oscillations and while the present units seem satisfactory, further work may be required.

The low frequency VCO's use high capacitance hyperabrupt tuning varactors which have shallow, large area junctions and are subject to "popcorn" noise caused by surface defects. The noise can be observed both on the oscillator RF spectrum and as fluctuations in diode reverse leakage current. A test procedure based on dc leakage current is necessary to screen out bad devices.

One unit (S/N 1) showed some lockup difficulties above 200 MHz, a problem attributed to slightly poorer carrier suppression in the SSB reference signal. It was occasionally necessary to rotate the bandswitch out of and back into the upper range to get lockup, but once locked there were no problems. This difficulty may also require further work.

The only other problem area was short bursts of unlocking at certain generator frequencies on the lowest ranges. This was traced to the pickup of quasi-coherent pulsed noise by the reference comparator.

OSLO S/N 0

DATE 7/13/76

LOCK RANGES
(MHz)

Range	Minimum	Maximum
125-220	114	239
75-140	64	151
45-85	40	91
28-52	26	60
17-32	16	36
11-20	10	22
7-13	7.0	14
5-9	5.0	10
3.2-6	3.0	6.9
2-3.7	2.0	3.9
1.3-2.3	1.0	2.9
0.8-1.5	0.68	1.9

FIGURE 5.1

OSLO S/N 1

DATE 7/14/76

LOCK RANGES
(MHz)

Range	Minimum	Maximum
125-220	109	232
75-140	65	154
45-85	39	91
28-52	26	59
17-32	15	34
11-20	9.2	23
7-13	6.2	14
5-9	4.6	11
3.2-6	2.6	6.8
2-3.7	1.7	3.8
1.3-2.3	1.2	2.3
0.8-1.5	0.68	1.5

FIGURE 5.2

OSLO S/N 2

DATE 7/13/76

LOCK RANGES
(MHz)

Range	Minimum	Maximum
125-220	110	235
75-140	66	161
45-85	40	92
28-52	27	61
17-32	15	34
11-20	9.4	23
7-13	6.4	12
5-9	4.3	9.1
3.2-6	2.7	6.4
2-3.7	1.7	3.8
1.3-2.3	1.2	2.2
0.8-1.5	0.69	1.5

FIGURE 5.3

The problem was temporarily solved by bandwidth reduction, but an improved board layout should offer an even better cure.

The single most important requirement of the Offset LO, that of low generator frequency leakage, appears to be met without difficulty. The results of leakage measurements using the Offset LO with a Tracking Servo Bridge Detector are shown in Figures 5.4 through 5.6. No leakage was observed that could be directly attributed to the Offset LO. The results for S/N 2, which showed no detectable leakage at 220 MHz, give a calculated relative generator component level on the LO output of better than 110 dB down.

No really accurate direct measurement of the generator leakage level has been made, but the important thing is that the desired result has been obtained: the LO leakage does not limit the performance of the detector.

At certain low frequencies there occurs spurious harmonic intermodulation components which are unfilterable by the lock loop. Measurements of these spurious levels are shown in Figures 5.7 through 5.9. They are believed to be of no real concern. These spurs cannot, by themselves, cause a spurious receiver response and their contribution to the receiver noise figure is completely negligible.

Other RF parameters of the LO units are shown in Figure 5.10 through 5.12. The input sensitivity is adequate and input level changes have no effect on the output signal.

The LO output properly drives the detector. The harmonic distortion of the LO output increases at the low frequency end, but does not cause any problems in the detector.

The power consumption of the Offset LO is within the limits provided by the Tracking Servo Bridge Detector except for the -5.2V supply current which exceeds the 0.7A spec by about 0.15A. It will be necessary to make a simple modification in the existing detectors to increase the current limit value on this supply. A modification kit for this purpose has already been supplied to ECOM. Power consumption charts are shown in Figures 5.13 through 5.15. The total ac input power to the TSBD/OSLO is about 55 Watts at 110 Vac line.

LEAKAGE TEST

OSLO S/N 0
TSBD S/N 15

Date 7/27/76

f_{Gen}, MHz	OSLO Range, MHz	Leakage, div	Noise, div
0.8	0.8-1.5	Not Detectable	± 3
1.0	0.8-1.5	"	"
2.0	1.3-2.3	"	"
3.0	2-3.7	"	"
5.0	3.2-6	"	"
7.0	5-9	"	"
10	7-13	"	"
15	11-20	"	"
20	17-32	"	"
30	17-32	"	"
50	28-52	"	"
70	45-85	"	"
100	75-140	"	"
130	75-140	"	"
150	125-220	"	"
180	125-220	"	"
200	125-220	5	"
220	125-220	3	"

Test Conditions: GR 1062 Source. Gain Adj. for -120 dBm = 12 div non-exp. Readings on exp scale.

FIGURE 5.4

LEAKAGE TEST

OSLO S/N 1
TSBD S/N 15

Date 7/22/76

f_{Gen}, MHz	OSLO Range, MHz	Leakage, div	Noise, div
0.8	0.8-1.5	2	± 3
1.0	0.8-1.5	3	"
2.0	1.3-2.3	Not Detectable	"
3.0	2-3.7	"	"
5.0	3.2-6	"	"
7.0	5-9	"	"
10	7-13	"	"
15	11-20	"	"
20	17-32	"	"
30	17-32	"	"
50	28-52	"	"
70	45-85	"	"
100	75-140	"	"
130	75-140	"	"
150	125-220	"	"
180	125-220	"	"
200	125-220	5	"
220	125-220	3	"

Test Conditions: GR 1062 Source. Gain Adj. for -120 dBm = 12 div non-exp. Readings on exp scale.

FIGURE 5.5

LEAKAGE TEST

OSLO S/N 2
TSBD S/N 15

Date 7/21/76

f_{Gen}, MHz	OSLO Range, MHz	Leakage, div	Noise, div
0.8	0.8-1.5	Not Detectable	±3
1.0	0.8-1.5	"	"
2.0	1.3-2.3	"	"
3.0	2-3.7	"	"
5.0	3.2-6	"	"
7.0	5-9	"	"
10	7-13	"	"
15	11-20	"	"
20	17-32	"	"
30	17-32	"	"
50	28-52	"	"
70	45-85	"	"
100	75-140	"	"
130	75-140	"	"
150	125-220	"	"
180	125-220	"	"
200	125-220	"	"
220	125-220	"	"

Test Conditions: GR 1062 Source. Gain Adj. for -120 dBm = 12 div non-exp. Readings on exp scale.

FIGURE 5.6

OSLO S/N 0

DATE 7/23/76

LF SPURIOUS LEVELS

(Spurious sidebands on LO output as a result of harmonic intermodulation products between $(f_{Gen} + f_{offset})/2$ and $N \cdot f_{offset}/2$ which lie inside loop bandwidth. Tests are made at spot frequencies near bottom of LF ranges which result in ± 1 kHz spurs.)

f_{Gen} kHz	Spurious Level dBC
802	-57
1362	-56
2002	-53
3202	<-65
5042	<-65

FIGURE 5.7

OSLO S/N 1

DATE 7/23/76

LF SPURIOUS LEVELS

(Spurious sidebands on LO output as a result of harmonic intermodulation products between $(f_{Gen} + f_{offset})/2$ and $N \cdot f_{offset}/2$ which lie inside loop bandwidth. Tests are made at spot frequencies near bottom of LF ranges which result in ± 1 kHz spurs.)

f_{Gen} kHz	Spurious Level dBC
802	-53
1362	-53
2002	-58
3202	<-65
5042	<-65

FIGURE 5.8

OSLO S/N 2

DATE 7/23/76

LF SPURIOUS LEVELS

(Spurious sidebands on LO output as a result of harmonic intermodulation products between $(f_{Gen} + f_{offset})/2$ and $N \cdot f_{offset}/2$ which lie inside loop bandwidth. Tests are made at spot frequencies near bottom of LF ranges which result in ± 1 kHz spurs.)

f_{Gen} kHz	Spurious Level dBC
802	-50
1362	-51
2002	-58
3202	<-65
5042	<-65

FIGURE 5.9

OSLO S/N 0

DATE 7/20/76

RF LEVEL AND DISTORTION

f_{Gen}, MHz	OSLO Range, MHz	Input Level Limits, dBm Min	Input Level Limits, dBm Max	Output dBm	Harm. Dist., dB down X2	Harm. Dist., dB down X3
0.8	0.8-1.5	-7	>+20	+10.6	18	34
2	1.3-2.3	"	"	+10.8	15	30
3	2-3.7	"	"	+11.0	14	26
5	3.2-6	"	"	+10.3	21	29
7	5-9	"	"	+10.3	22	30
10	7-13	"	"	"	23	34
15	11-20	-6	"	+10.2	25	"
25	17-32	"	"	"	"	"
50	28-52	-5	"	+10.0	27	32
70	45-85	-4	"	+9.6	29	35
100	75-140	-3	"	+9.0	31	37
150	125-220	-1	"	+9.6	"	"
220	125-220	+2	"	+10.0	22	36

FIGURE 5.10

OSLO S/N 1

DATE 7/23/76

RF LEVEL AND DISTORTION

f_{Gen}, MHz	OSLO Range, MHz	Input Level Limits, dBm Min	Input Level Limits, dBm Max	Output dBm	Harm. Dist., dB down X2	Harm. Dist., dB down X3
0.8	0.8-1.5	-7	>+20	+10.3	20	33
2	1.3-2.3	"	"	"	19	"
3	2-3.7	"	"	"	21	36
5	3.2-6	"	"	+10.2	23	34
7	5-9	"	"	+10.1	24	"
10	7-13	-6	"	"	"	35
15	11-20	"	"	"	25	"
25	17-32	"	"	+10.0	26	"
50	28-52	-5	"	+9.8	27	"
70	45-85	-4	"	+9.6	"	"
100	75-140	-1	"	+9.4	26	36
150	125-220	+1	"	+9.1	34	34
220	125-220	+6	"	+9.4	23	"

FIGURE 5.11

OSLO S/N 2

DATE 7/21/76

RF LEVEL AND DISTORTION

f_{Gen}, MHz	OSLO Range, MHz	Input Level Limits, dBm Min	Input Level Limits, dBm Max	Output dBm	Harm. Dist., dB down X2	Harm. Dist., dB down X3
0.8	0.8-1.5	-7	>+20	+10.4	15	32
2	1.3-2.3	"	"	"	22	37
3	2-3.7	"	"	"	21	36
5	3.2-6	"	"	+10.4	24	34
7	5-9	"	"	+10.3	24	34
10	7-13	-6	"	+10.3	24	35
15	11-20	"	"	+10.3	25	35
25	17-32	-5	"	+10.2	26	34
50	28-52	-4	"	+9.9	27	33
70	45-85	"	"	+9.9	"	"
100	75-140	-3	"	+9.8	24	36
150	125-220	0	"	+9.8	29	35
220	125-220	+4	"	+9.8	22	33

FIGURE 5.12

OSLO S/N 0

DATE 7/23/76

POWER CONSUMPTION CHART

Section	Supply Currents, mA				Power, mW
	-22	-5.2	-18	+18	
Entire VCO Module	110*				2420
Offset Source			10	48‡	1044
SSB Processor		370			1924
ϕ-F Detector	14△	350			2128
Loop Filter	13				286
Isolation Amp	15	86			777
TOTALS	152	806	10	48	8579

* Inc. LPF & Filter Switching ckts

‡ Inc. Ref. Comp. Pos. Supply

△ In Lock

FIGURE 5.13

OSLO S/N 1

DATE 7/22/76

POWER CONSUMPTION CHART

Section	Supply Currents, mA				Power, mW
	-22	-5.2	-18	+18	
Entire VCO Module	115*				2530
Offset Source			12	44‡	1008
SSB Processor		380			1976
ϕ-F Detector	14△	340			2076
Loop Filter	16				352
Isolation Amp	14	84			745
TOTALS	159	804	12	44	8687

* Inc. LPF & Filter Switching ckts

‡ Inc. Ref. Comp. Pos. Supply

△ In Lock

FIGURE 5.14

OSLO S/N 2

DATE 7/13/76

POWER CONSUMPTION CHART

Section	Supply Currents, mA				Power, mW
	-22	-5.2	-18	+18	
Entire VCO Module	119*				2618
Offset Source			10	36∓	828
SSB Processor		380			1976
ϕ-F Detector	15△	340			2098
Loop Filter	12				264
Isolation Amp	15	88			330
TOTALS	161	808	10	36	8114

* Inc. LPF & Filter Switching ckts

∓ Inc. Ref. Comp. Pos. Supply

△ In Lock

FIGURE 5.15

5. Test Results (continued)

No environmental testing has been done on any of the Offset LO units. While no difficulties are expected, some testing would be desirable before a production lot is built, particularly temperature tests.

A mockup of the Offset LO was subjected to vibration testing during the initial design. While no problems were encountered with the basic structure some minor work may be required on cable supports. The unit does not contain any components (such as meters) that are sensitive to shock and vibration. All tuned circuits use toroidal inductors.

Materials and finishes have been selected for acceptable humidity tolerance, based on experience with the detector unit. There are no critical high-impedance circuits.

No trouble is expected with LO operation over the +15 to +45°C ambient temperature range. Similar circuits were temperature tested in the TSBD and the single range demonstration LO unit. More effort may be required to design a better means of heat-sinking the high power ECL flat pack devices. The present units have small convectors, plus a post to conductively sink them to the housing covers. The devices have a case temperature of about +65°C in a unit operating at room temperature.

Figure 5.16 shows the actual offset frequency for each unit. The offsets are well within the lock range of the IF reference section of a Tracking Servo Bridge Detector.

OFFSET FREQUENCY

OSLO S/N	DATE 1976	OFFSET ERROR ppm	CONDITIONS
0	7/23	+6	Warmed up in cabinet at bottom of TSBD
1	7/22	-21	Warmed up in cabinet at bottom of TSBD
2	7/22	-14	Warmed up in cabinet at bottom of TSBD

FIGURE 5.16

6. CONCLUSIONS

These Offset LO units have proven the feasibility of the design approach. The units operate over the full 0.8-220 MHz range and meet the requirements for use with the Tracking Servo Bridge Detector. The method used for producing the Offset LO signal, generation of a SSB reference signal at half frequency followed by active filtration by a phase lock loop, seems entirely satisfactory for the application. In particular, the level of generator leakage is generally undetectable and in no case limits the performance of the detector. This represents a considerable technical accomplishment.

There remains, however, a fair amount of design "cleanup" work which must be done before Offset LO units can be produced. Nearly every etched circuit board needs some revision, some mechanical and assembly drafting work is needed and there are a few loose ends concerning the electrical performance. Some environmental testing also needs to be done.

An important part of the program to implement precision bridge-type crystal measurements has been accomplished now that a design has been proven for the Offset LO unit. No serious difficulties should be encountered in building production units for use with the Tracking Servo Bridge Detector.

Section II

AUTOMATIC MICROCIRCUIT BRIDGE

7. INTRODUCTION

7.1 General

This section of the report describes a paper study of a proposed microcircuit bridge for use in an automated system for measurement of the parameters of quartz-crystal resonators. The study was based on experimental work done by ECOM in the Frequency Control and Signal Processing Area and follows the guidelines entitled, "Automatic Microcircuit Bridge," dated 12 February 1975. The first experimental model was provided to GR for "hands-on" operation and to evaluate the "Relcom" bridge transformer system. Three sample varactor chips were also supplied for evaluation of leakage and the control characteristics.

This study analyzes possible sources of measurement errors and suggests corrective methods and construction details for the next development bridge model. Further development work on the bridge has been performed by GenRad under ECOM Contract DAAB07-76-C-1380. The contract also authorized the design of an automatic balancing unit to interface the bridge with the Tracking Servo Bridge Detector. The results of bridge development and balancing unit design will be reported as part of the ECOM contract.

7.2 Complete Measurement System

Figure 7.1 is a block diagram showing the elements required for automatic measurement of the parameters of quartz resonators. While it is possible to make a fully automated system, the use of some manual set-up adjustments is probably most cost effective.

The system must be able to make and store initial-balance settings before the device under test is connected and must provide the proper phase adjustment of the servo bridge detector so the corresponding outputs will properly control the resistive and reactive balancing of the bridge. The basic readouts required are the Frequency and Resistance of the resonator under test with a secondary measurement of Q or L. The secondary readout is derived by measuring the change in resonant frequency as a result of a capacitance-balancing offset. Q and L could possibly be automatically obtained and displayed using the computational ability of a digital microprocessor.

7.3 Major Areas of Investigation Required

7.3.1 Residual Bridge Parameters and Effect on Measurements

1. Stray L and C in circuit.
2. Q of and reverse leakage in varactors..
3. Varactor feed circuits and compensation.
4. Detector coupling efficiency.
5. Non-linear varactor voltage characteristics and effects of high RF drive levels.

7.3.2 Readout Errors

1. Due to control voltage to G and C conversion.
2. Effect of temperature on above.
3. Accuracy of possible high-frequency corrections via microprocessor.

7.3.3 Use of Digital Microprocessor

1. To obtain desired direct readout (to subtract initial and final balance values and take reciprocal of G_x to read out R_{xp}).
2. To correct for errors.

7.3.4 Servo Problems

1. Loop stabilization and settling time.
2. System for automatic setting of servo bridge detector phase. Loop stabilization and settling times as well as the possible servo system for setting the phase shifter in the servo bridge detector have not been considered in any detail in this study.

8. DETAILED CIRCUIT STUDY

8.1 Schematic

Figure 8.1 shows the proposed bridge configuration with parameters chosen to cover the required measurement range with the capacitance range available from suitable chip varactors. A single varactor chip is used for C1 and four in parallel for C4. The use of parallel varactors minimizes the parasitic inductance in C4 and available chips of the values chosen have twice the Q of those with double the capacitance. Physically there is adequate space on top of the associated blocking capacitor for four chips.

It would be desirable to use higher bridge resistor values to minimize the effect of parasitic inductance and improve resolution when measuring higher valued "unknowns". The values shown are necessary when using high-Q abrupt junction varactors which have capacitance control ranges of the order of 3 to 1. Recently some high-Q, high-voltage, hyperabrupt-junction varactors have become available with 7 to 1 capacitance control ranges which makes a 4 to 1 increase in the bridge resistors values possible. The use of these should be seriously considered.

8.2 Chip Varactor Diodes

It is proposed that the varactor chips be bought to available $\pm 2\%$ tolerance to minimize the spread in calibration that must be provided. Low reverse leakage is essential and if it is not possible to purchase to desired limits, units as received will have to be tested and those outside acceptable limits discarded for this use. Varactors from a given lot are quite likely to have similar leakage characteristics so sampling checks may be satisfactory.

8.3 Unbalance Due to Resistance Balancing Varactor Feed Circuit

C8 and R5 introduce a leading phase shift at the low end of the frequency range which must be corrected by increasing C4 initial balance setting. A compensation scheme was devised which introduced the same RC phase lead in

the opposite arm of the bridge but was abandoned in favor of increasing the range of C4 to provide for the offset in addition to the required measurement range. With the values shown on the schematic the offset amounts to less than 10pF at 0.8MHz while a total range of plus and minus 60pF is provided. Analysis shows that very good low-frequency compensation could have been provided by the added elements but they would have added some undesirable parasitic inductance with serious effects on the high frequency performance.

8.4 Bridge Output-Transformer Limitations

The characteristics of the output transformer can seriously limit the performance of the bridge. Of principal concern is the common-mode coupling of the output transformer. This is due to unbalanced coupling in the transformer which produces an output to the detector even though the bridge itself is perfectly balanced. The full voltage across the "unknown" is applied to both input terminals of the output transformer at balance while the desired output signal is due to the voltage between the input terminals which is a very small fraction of the former for the resolution desired.

In the first models of the bridge three "Relcom BT8C", 200- to 50-ohm transformers are cascaded to produce the output transformer. Figure 8.4.1 shows the circuit configuration and measured interwinding capacitances. The common-mode rejection is produced by cancellation of the capacitive coupling in the grounded center-tapped windings of the two transformers nearest the detector. The scheme depends on the lack of significant leakage inductance and resistance in the center-tapped windings, since any voltage to ground is capacitively coupled to the detector. Figure 8.4.2 shows the measured common-mode coupling. Figure 8.4.3 shows the measured normal output coupling under the worst case condition when the bridge is set to balance an "unknown" resistance of 2 ohms. The coupling factor was measured by simulating the bridge output impedance with a series 58pF capacitance which represents the approximate equivalent circuit when balancing 2 ohms.

With the bridge impedances shown on the schematic at 0.8MHz, a capacitance change of 1pF across "unknown" terminals produces a quadrature voltage of 5.18×10^{-6} times the "unknown" voltage when measuring a 2-ohm resistance. The coupling factor from Figure 5 is 1.85×10^{-2} so this produces a voltage of 9.6×10^{-8} times "unknown" voltage into a 50-ohm detector. Figure 4 shows that the common-mode coupling produces 7.25×10^{-7} times "unknown" voltage into the same detector. Depending on the relative phase of the two voltages this could represent up to a 7.6pF capacitance error (7.6 X unbalance voltage for 1pF). A better output transformer is indicated. There is a good possibility that a miniature triple-shielded transformer can be built giving a 20dB or greater improvement in the ratio of desired to common-mode coupling. It is also essential that the actual connections to the transformer from the desired points in the bridge be arranged to produce no extraneous coupling to r-f currents in the bridge elements or the true balance condition will not be observable.

8.5 Detector Sensitivity Limitation on Measuring Accuracy

With the "Relcom" output transformer system, a capacitance offset of 1pF produces 9.6×10^{-8} times the "unknown" voltage into the detector when

measuring a 2-ohm resistance at 0.8MHz. With 0.1V across the "unknown" this is a voltage of 9.6×10^{-9} across 50 ohms or -147dBm. Changing the output transformer turns ratio from 2-to-1 to 3-to-1 as shown on schematic will give a 3.5dB improvement but it looks like ±1pF is about the safe measuring resolution limit set by the detector under worst case conditions at this RF level. The corresponding limit for parallel resistance is ±200K ohms. The capacitance-measuring resolution improves as the square of the frequency in terms of C, and the resistance-measuring resolution directly with frequency up to 10MHz then gradually flattens and turns down above 40MHz, as limited by detector sensitivity (the drop above 40MHz is not thought to be significant compared to other probably high-frequency errors).

8.6 Maximum RF Drive Limitation

Figure 8.6.1 shows the measured increase in effective capacitance of the chip varactor diode, at increased applied RF levels, above the capacitance measured with 141 millivolts applies. 141 millivolts is thought to be sufficiently low to give the true incremental capacitance over the entire control range of the varactor.

Figure 8.6.2 shows the approximate errors in the indicated values of the parallel resistance of the "unknown", R_{xp}, relative to its actual values. The maximum power level to the "unknown" was determined by limiting the applied r-f voltage to the resistance-balancing varactor to 0.707 volts at initial balance. Forward conductance of the varactor does not permit the initial balance to be made at significantly higher than 1Vrms at the minimum control voltage and 0.707V is already seriously increasing the effective capacitance. The measuring error of R_{xp} is shown for this maximum power level as well as could be determined from a linear extrapolation of the curves of Figure 8.6.1. The 0.707 volt curve becomes extremely steep near intial balance and extrapolation for higher values impossible. This, with the ±.01pF readability of the curves, makes the error determination for measured resistances greater than 50 ohms impractical, but at this point the error has reached 14 percent. The resistance measuring error at 1/4 the maximum power level is also shown and, while the ability to read and extrapolate the curves still limits the accuracy of the determination, the errors seem quite acceptable over the R_{xp} ranges shown.

The parallel capacitance measuring accuracy is also adversely affected by increased r-f drive level. The effect is to make a given capacitance offset require larger capacitance change at "unknown" terminals to restore the balance. The approximate error in the measured capacitance, C_{xp}, is shown in Figure 8.6.3 with 1/4 the maximum power into the "unknown".

For errors caused by the non-linearity in the varactors for both R and C measurements, it would appear that the practical limit would be the 1/4 power level shown in the curves which means that the actual maximum power into the "unknown" would decrease from 9 milliwatts with R_{xp} = 2 ohms to 1.3 milliwatts at R_{xp} = 100 ohms, and 0.14mw at R_{xp} = 1KΩ. As a practical matter, maximum specification of 300 millivolts across the "unknown" should meet the accuracy requirements for all values of R_{xp}, and if this level is set with the "unknown" connected, the voltage for initial balance will be within acceptable limits for the measurement.

9 RESISTANCE AND CAPACITANCE READOUT

9.1 General

The values of connected "unknown" parallel resistance and capacitance are determined from the initial and final balance capacitance settings of the varactors in the bridge which in turn are functions of the applied control voltages. Not only are the relationships between voltage and capacitance nonlinear but these relationships are affected by the temperature of the varactors. The readout scheme must therefore provide for the required linearization as well as temperature compensation over the required operating range of the bridge. The readouts from the differences between initial and final balance values give the capacitance and conductance values of the unknown. Readout in terms of parallel resistance requires further reciprocal processing of the conductance value.

9.2 Resistance Readout

Figure 9.2.1 shows the nominal voltage required for various values of R_{xp} and the nominal deviation in voltage that must be resolved to determine resistance value to within 5%. Individual varactor diodes will have slightly differing characteristics so that individual calibration will be required for each bridge assembly to provide the direct resistance readout desired. Note that the voltage increment for a 5% resistance change becomes quite small at the higher values and the situation would be hopeless if it were not for the fact that an initial balance is made before the "unknown" is connected and then the difference between this and the final balance used to determine the value of the connected parallel "unknown" resistance. What really is determined is:

$$\frac{1}{R_{xp}} = \frac{C2}{R3}\left(\frac{1}{C_1\text{-}2} - \frac{1}{C_1\text{-}1}\right)$$

C_1-1 and C_1-2 are the initial and final balance values of C_1, respectively.

Figure 9.2.2 is a possible scheme for obtaining the desired direct parallel resistance readout consisting of the following: An auxiliary varactor diode is placed in the same temperature environment with the bridge and supplied with a constant current fixed frequency signal. The control voltage to the resistance balancing input of the bridge is also applied to an adjustable gain, adjustable offset d-c amplifier whose output supplies the control to the auxiliary diode. These adjustments provide the means for making the capacitance of the auxiliary diode closely track that of the bridge resistance balancing varactor over its entire control range, and since the diodes are in the same temperature environment this condition should be maintained over the desired temperature range. The resulting signal voltage across the auxiliary diode is proportional to $1/C_1$ so the difference between the initial and final balance is $1/R_{xp}$. The actual gain and bias adjustments might better be provided with pure resistance elements to eliminate possible d-c amplifier drift.

It is proposed that a digital microprocessor be used to subtract initial and final values with an appropriate scale factor and take the reciprocal to provide a direct display of R_{xp} in ohms.

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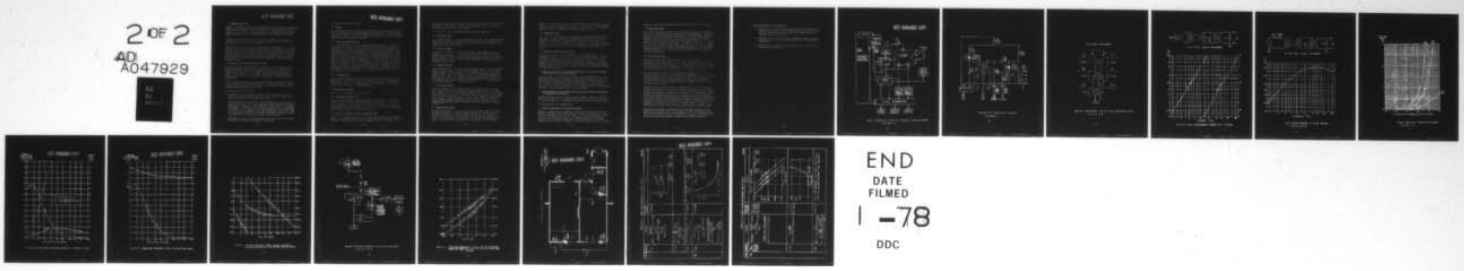

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9.3 Capacitance Readout

Figure 9.3.1 shows the nominal voltages required for various parallel capacitance values and the nominal deviation in voltage that must be resolved to determine the value to within 0.1pF. The situation in regard to resolution is not quite as critical as for R_{xp} measurement but it is essential that the difference between the initial and final balance values be taken to determine C_{xp}.

A scheme similar to that used for the resistance readout may be used for capacitance but in this case no reciprocal operations are necessary to give an indication proportional to capacitance.

It is not certain if this scheme is justified for this readout. Analog linearization and simple temperature compensation may be satisfactory. A microprocessor is useful for subtracting the initial and final balance values for direct display of C_{xp} in picofarads and it may be possible to include temperature information obtained from a sensor on the bridge assembly to correct the displayed value over the desired temperature range. Further study will be required to see if this is the best way to obtain the readout within the accuracy desired.

10. ANALYSIS OF POSSIBLE HIGH FREQUENCY ERRORS

A number of residual parameters have a large effect on the accuracy of measurement and initial balance shifts particularly at the higher frequencies. Series inductance is the most important residual because of the very low impedance level ($\approx$4 ohms) of the bridge arms and the small capacitance range. It is difficult to keep residual inductance of connections below 1 nanohenry which produced a reactance of somewhat over 1 ohm at 220MHz (See Appendix A).

It does not appear practical to reduce the residuals sufficiently to keep the error in direct-reading measurements within the desired accuracy and either corrections must be applied to the results or some method of automatically correcting the indications must be used.

The most important residuals are:

1. Inductance in the connection to the UUT. This inductance, even if a fraction of a nanohenry will have a very large effect on R and C at the higher frequencies if the measured R is small.

2. Inductance in the resistance arm. This inductance will cause a shift in the initial balance point of the capacitance measuring varactor which is independent of frequency. There is also an error in the measured capacitance which is a function of the measured resistance which is independent of frequency. This inductance can be compensated by a shunt capacitance but with the low resistance, a very large capacitance is required. There is a possibility that this error can be compensated by adding a resistor in series with the capacitor in the fixed capacitance arm.

3. Inductance and loss in the varactors and connections also causes significant errors in measured resistance and capacitance.

11. CRITICAL CONSTRUCTION DETAILS

11.1 General

The chip varactor diodes as well as any components connected to their cathodes must be protected from any contamination which could cause current leakage. It is also essential that light be excluded from the diodes to prevent photoconduction. Hermetic sealing of at least the portion of the bridge containing these elements is therefore recommended.

11.2 Precision Bridge Resistors

It is recommended that thin-film tantalum nitride resistors be used for the major-low-value bridge resistors, adjusted to value by high temperature oxidation. These resistors must have extremely low parasitic inductance and low coupling to one another as well as other portions of the bridge. It is recommended that these resistors be placed on the ceramic window of a metal cavity containing the varactor chips, chip capacitors and high valued resistors, with a direct connection to a sealed "unknown" terminal through this window. A three dimentional arrangement of the resistors may be more desirable to reduce some undesired coupling but it is essential not to add any parasitic inductance in any of the connections. Laser trimming of the resistors in the complete assembly to calibrate the bridge for variations in the capacitive elements may be used but is not thought to be essential since it is expected that some adjustment can be provided in the readout system. If hyperabrupt varactors are found to be satisfactory higher valued resistors will reduce some of the problems.

11.3 Chip Capacitors

High temperature stability, high Q, chip capacitors must be used. C2 must be selected to produce 48.5pF within 1 percent in combination with parasitic capacitance. C6 and C8 are available in NPO ceramic cubes of suitable size in the values shown. It is recommended that all capacitors be recessed into milled cavities to minimize series inductance.

11.4 High-Value Resistors

R5 and R6 may be standard 5% chip resistors.

11.5 Bridge Output Transformer

The common-mode coupling of cascaded miniature transformers as used in the original model of the bridge seriously limits the performance. It is felt that a miniature-triple-shielded transformer can be designed to provide much better performance. The physical volume of such a transformer may be somewhat greater than the original arrangement, but it is felt that this approach is necessary to obtain the performance desired.

11.6 Series Load Capacitor and Terminal Connections

Details of the physical arrangement of the 20, 30, and 32pF series load capacitors must be carefully worked out to prevent addition of excessive series inductance between the quartz resonator under test and the measurement termi-

nals of the bridge. The only practical approach is to include these capacitors in separate interchangeable assemblies along with the connecting device. Extremely close tolerances on the capacitance values are specified so some adjustment means will have to be provided.

12. COMPARISON OF EXPECTED PERFORMANCE WITH ORIGINAL OBJECTIVES

12.1 Frequency Range

0.8 to 220MHz required. It would be difficult to extend this range appreciably. Output coupling problems are the principal limitation but the reactance balancing range is becoming extremely small at the lowest frequency with only a ±20pF capacitance balancing range.

12.2 Resistance Range

Less than 2 ohms to over 1 megohm desired. While the bridge can easily balance over the range of 2 ohms to infinity, the resolution and accuracy become increasingly poor at the higher values of R_{xp}. A practical limit of 5KΩ is probably as good as can be expected. Residual inductance in resistance balancing arm will limit low end of resistance range to perhaps 3 ohms at frequencies above 100MHz.

12.3 Capacitance Range

±20pF minimum desired. The total range provided by proposed circuit is ±60pF but some allowance must be made for initial balance offset. At the lowest frequency where the widest range is most important it is expected that the initial balance offset can be held to ±1pF if low frequency compensation is added, so most of the total range can be used. Without this compensation the offset with the circuit shown is 10pF so with a ±60pF range there should be no problem except that an offset in initial balance will be required as the frequency approaches the lower range limit.

12.4 Resistance Accuracy

±5% minimum desired. It is expected that this accuracy can be maintained from 2 ohms to over 200 ohms even at the lowest frequency with 1 mv across the "unknown". Due to the conductance measuring nature of the bridge, readout resolution becomes very poor at increasing values of R_{xp}, and it is estimated that it will be very difficult to resolve a value of 5KΩ within better than 50%, although it should be possible to detect the presence of 500KΩ at the lowest operating frequency with 100 millivolts across "unknown". High-frequency accuracy will depend on careful control of parasitic inductance. (See Par. 10)

12.5 Capacitance Accuracy

±0.1pF minimum desired. At the lowest operating frequency with the maximum available sensitivity of the servo-bridge detector it is estimated that, with 100 millivolts across the "unknown", ±1pF is about all that can be resolved by the detector. Above 2.5MHz it is expected that sufficient resolution for the desired ±0.1pF accuracy can be obtained at this drive level. If the drive level is increased to 300 millivolts it is expected

that the desired resolution can be obtained above 1.5 MHz, but with 1 millivolt drive it can only be obtained above 25 MHz. High-frequency accuracy depends on careful control of parasitic inductance. (See Par. 4) Further experimental study will be required to determine possible accuracy.

12.6 Temperature Range

-50 to +105°C. Good temperature compensation of the control characteristics and readout of the resistance and capacitance balancing varactors will be required to retain the desired measuring accuracy over this range. It is expected that this can be accomplished in the design of the readout system, the readout system for R_{xp} being the most critical, but it should be possible to keep errors from temperature variation comparable to those from other sources.

12.7 Drive Level Range (Across Unknown)

1mV to 1Vrms desired. Unless varators with considerably higher control voltages are used, the upper end of the range of voltages across the unknown will have to be restricted to about 300 millivolts or the resistance and capacitance measuring accuracy will be destroyed. At about 1 volt with present varactors the initial balance can no longer be made due to forward conduction of the varactor diodes on signal peaks. The capacitance-measuring accuracy limits the low end of drive range at the low end of frequency range as shown under paragraph 6.5.

12.8 Direct Readout of Resistance and Capacitance of "Unknown" as a Linear Function of Applied Control Voltage

This is possible for parallel capacitance but much more difficult for the resistance readout due to reciprocal nature of the measurement. $1/R_{xp}$ or the measured conductance can be made a linear function of the change in control voltage from the initial balance value, if desired. It is expected that the direct display of R_{xp} can best be provided by a digital microprocessor to give the desired readout. It is expected that the servo-problems although not insignificant can be successfully solved.

12.9 Initial Balance and Resistance and Capacitance Calibration Independent of Frequency and Temperature

Residual unbalance output at least 40dB below maximum unbalance is desired when either frequency or temperature is varied over the specified ranges. It is improbable that this can be accomplished over the entire frequency range.

13. RECOMMENDATIONS FOR FURTHER STUDY

13.1 Bridge Compensation for Parasitic Elements

There are probably some improvements possible by judicious addition of compensation elements to the bridge circuit. However, it is difficult to predict the performance tradeoffs that result. It is recommended that the next step in this investigation consist of building an assembly, using best available microcircuit techniques, based on best judgement as to physical configuration to minimize all parasitic impedances consistent with the design

objectives and experimental performance of the first models of the bridge.

13.2 Measurement Range

Part of the difficulty with the original circuit configuration stems from a very limited reactance-balancing range at the lower frequencies. A method was worked out for compensating the capacitance initial balance offset introduced by the resistance-varactor control feed circuit which preserved the available capacitor measurement range, but it was feared that the added elements would significantly reduce the high-frequency resistance measurement range due to added parasitic inductance. The better approach is to increase the capacitance-balancing range which is desirable, not only for the measurement of quartz resonators at the lower frequencies but also for other general impedance measurements. The practability of using four parallel capacitance balancing varactors in a suitable physical configuration in the assembly should be investigated.

13.3 Measurement Accuracy

Measurement accuracy depends on many factors besides the effect of parasitic impedances in the bridge circuit itself. It is assumed that the connecting specifications will standardize conditions external to the bridge which will probably introduce a reasonably small but fixed series inductance. This also can be corrected for by the microprocessor. There may be some problems with introduction of the series load capacitors that need to be resolved.

The sensitivity of the detector and the coupling efficiency of the bridge effect the resolution of the measurements and consequently set a limit on measuring accuracy. These effects have been estimated but need to be experimentally verified with an actual bridge output system. The sensitivity of the servo-bridge detector could be improved by reducing the bandwidth, but this will limit the response speed and must be considered in realtionship to required balancing times.

The major factor affecting measuring accuracy is the ability of the readout system to determine truly the initial and final balance values of varactor capacitances in the bridge from the respective control signals and to compute accurately the values to display. Due to requirement of storing the initial values, then subtracting final values to compute the values to display, it is felt that digital processing is more suitable than analog methods particularly since readout in parallel resistance requires a reciprocal operation in the process. Analog methods certainly are needed in the converting of control voltages in processing the readout including compensation for the effect of temperature on varactor characteristics. Further study is needed to find the most effective use of both methods for obtaining the required accuracy.

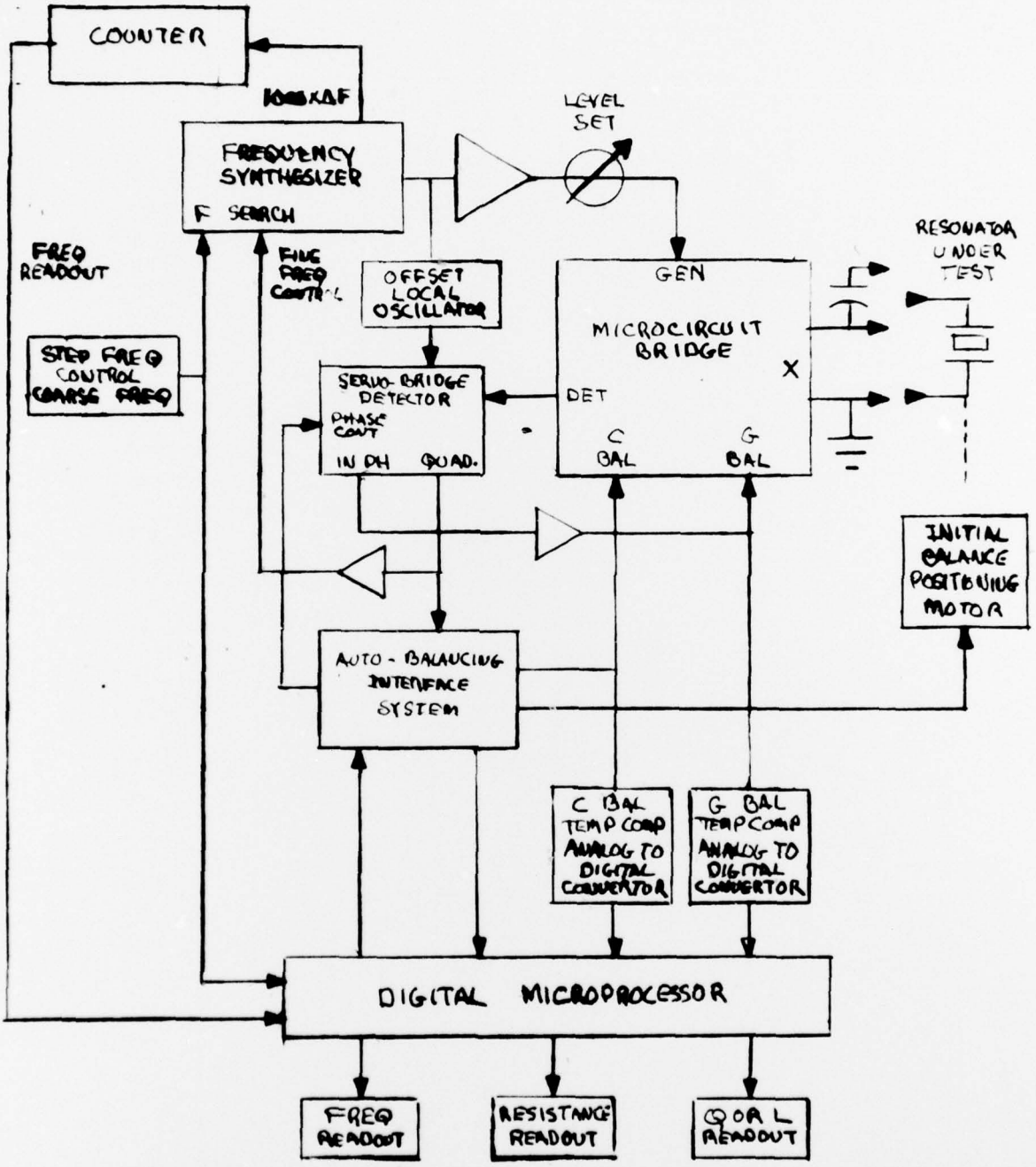
The problems with parasitic inductance in the resistance elements of the bridge will be greatly reduced if varactors with wider capacitance ranges can be obtained without other characteristics such as Q being degraded since the resistance values can then be substantially increased. This should also improve resolution and accuracy of higher valued unknown resistances.

13.4 Recommended Order of Investigation

1. Design and optimize the basic bridge assembly with measurements on experimental models to determine and minimize parasitic elements. Use higher valued resistors with wide control range hyperabrupt function varactors if possible.

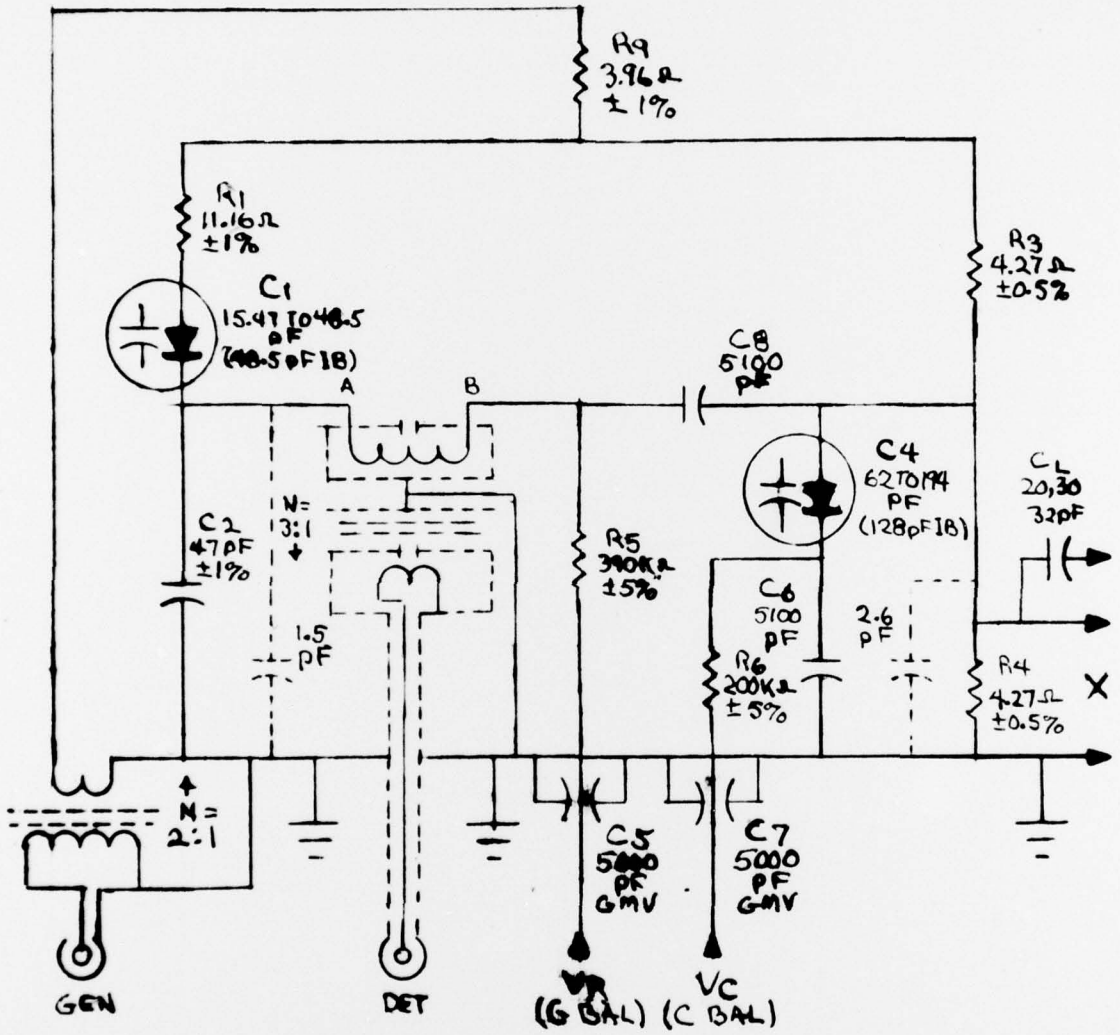
2. Develop a readout system including temperature compensation with consideration of any limitation this might have on auto-balancing servo system.

3. Resolve the servo problems for the complete system and model it to determine overall performance.



BLOCK DIAGRAM OF COMPLETE AUTOMATIC MEASURING SYSTEM

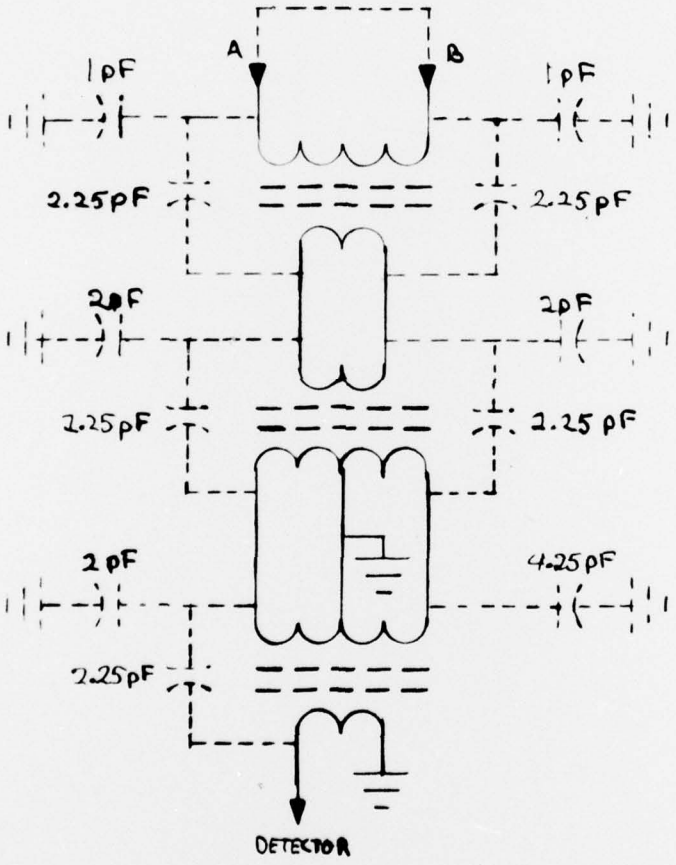
FIGURE 7.1



SCHEMATIC OF MICROCIRCUIT BRIDGE

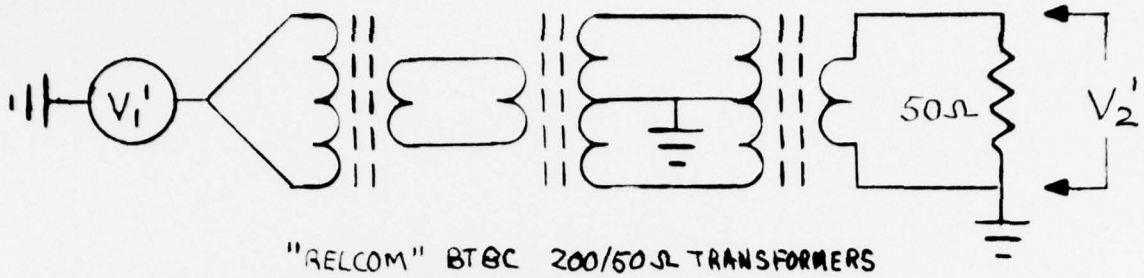
FIGURE 8.1

"RELCOM" BTBC TRANSFORMERS



PARASITIC CAPACITANCES "RELCOM" OUTPUT TRANSFORMER SYSTEM

FIGURE 8.4.1



"RELCOM" BTBC 200/50Ω TRANSFORMERS

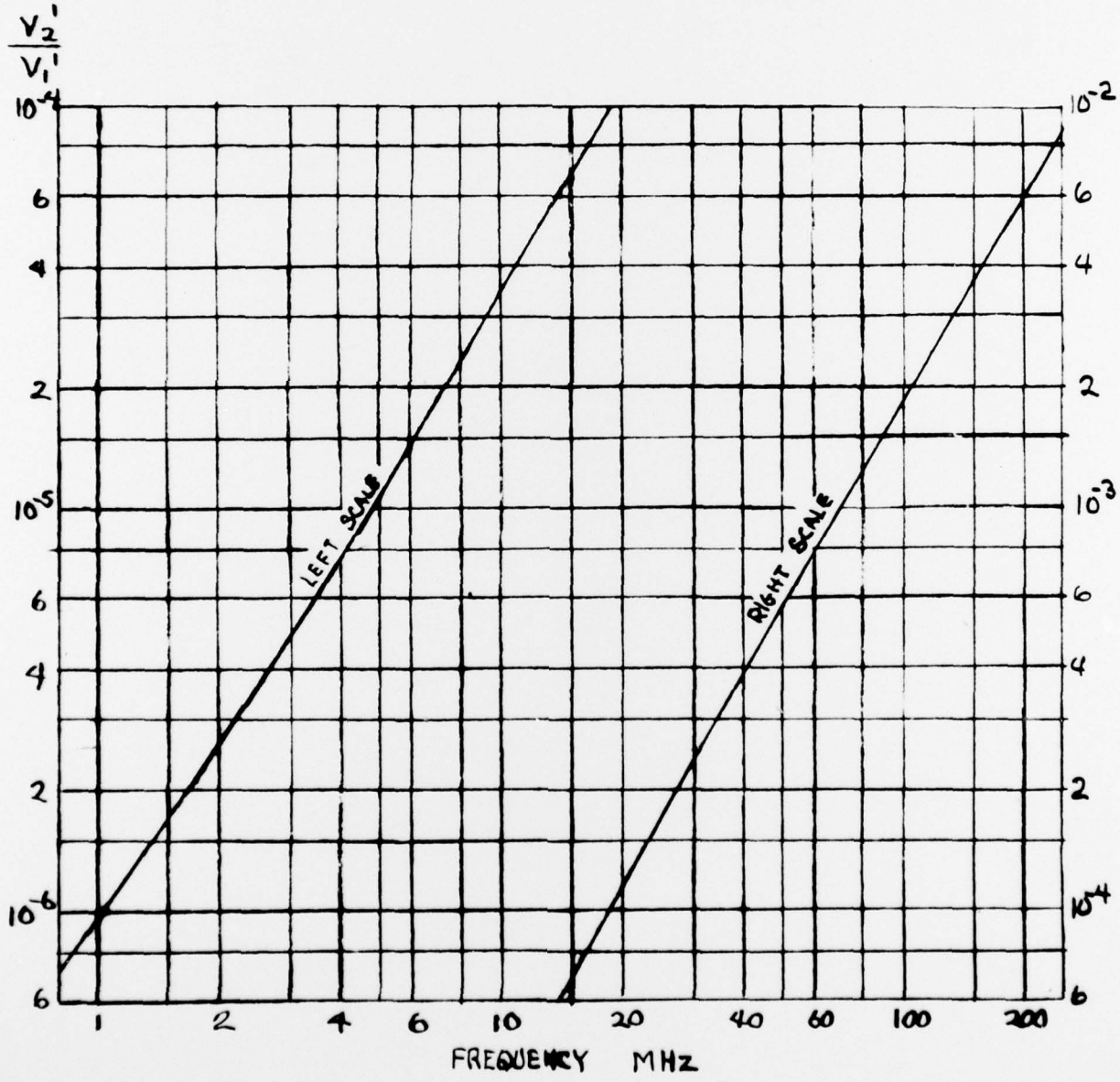
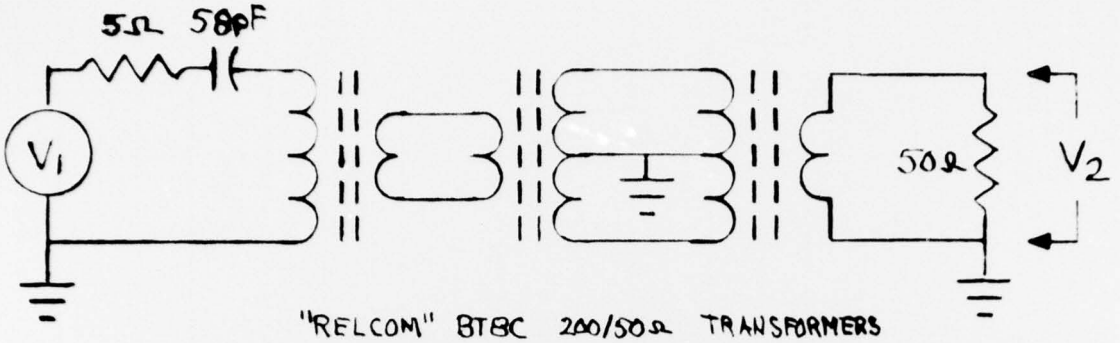
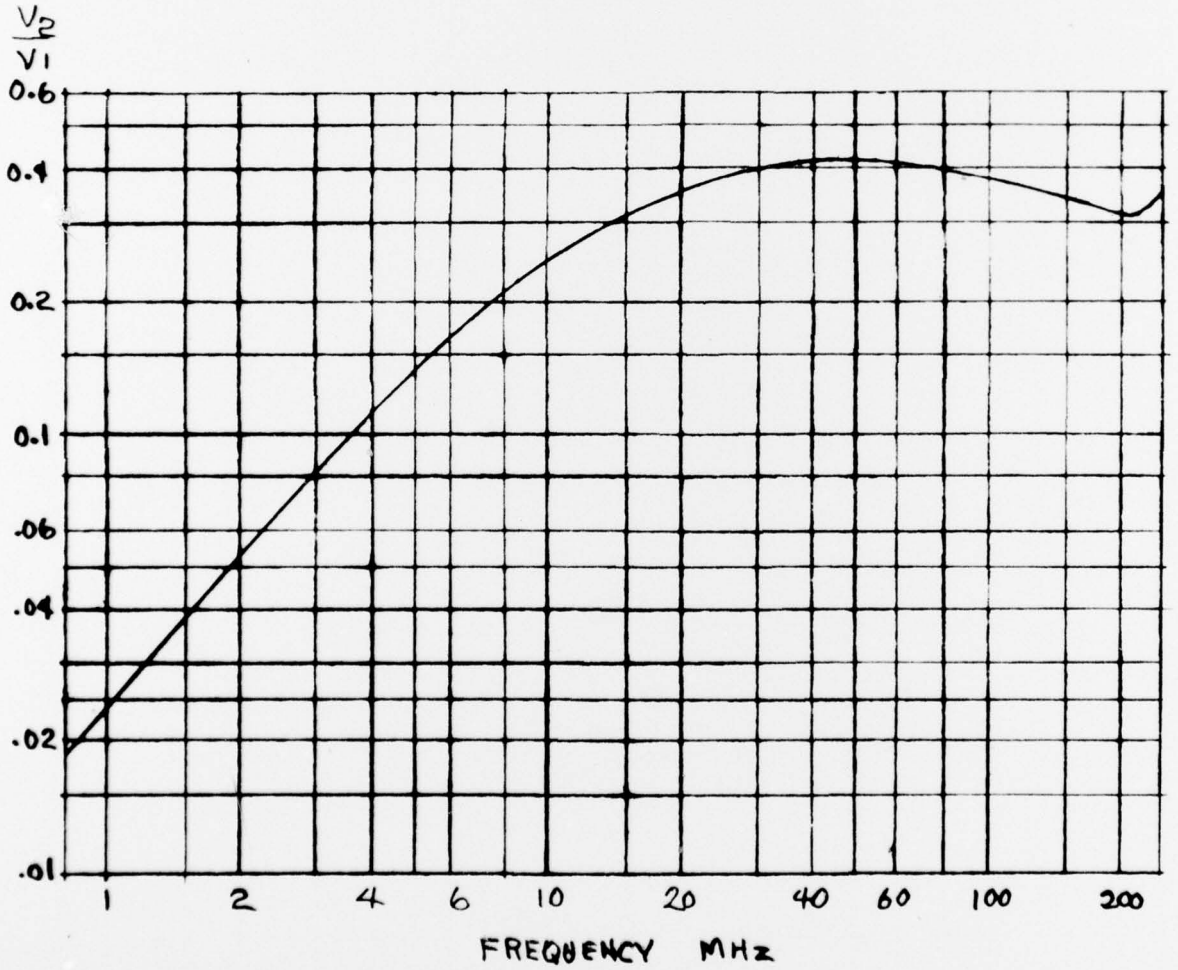


FIG. 8.4.2 BRIDGE TRANSFORMER COMMON-MODE COUPLING

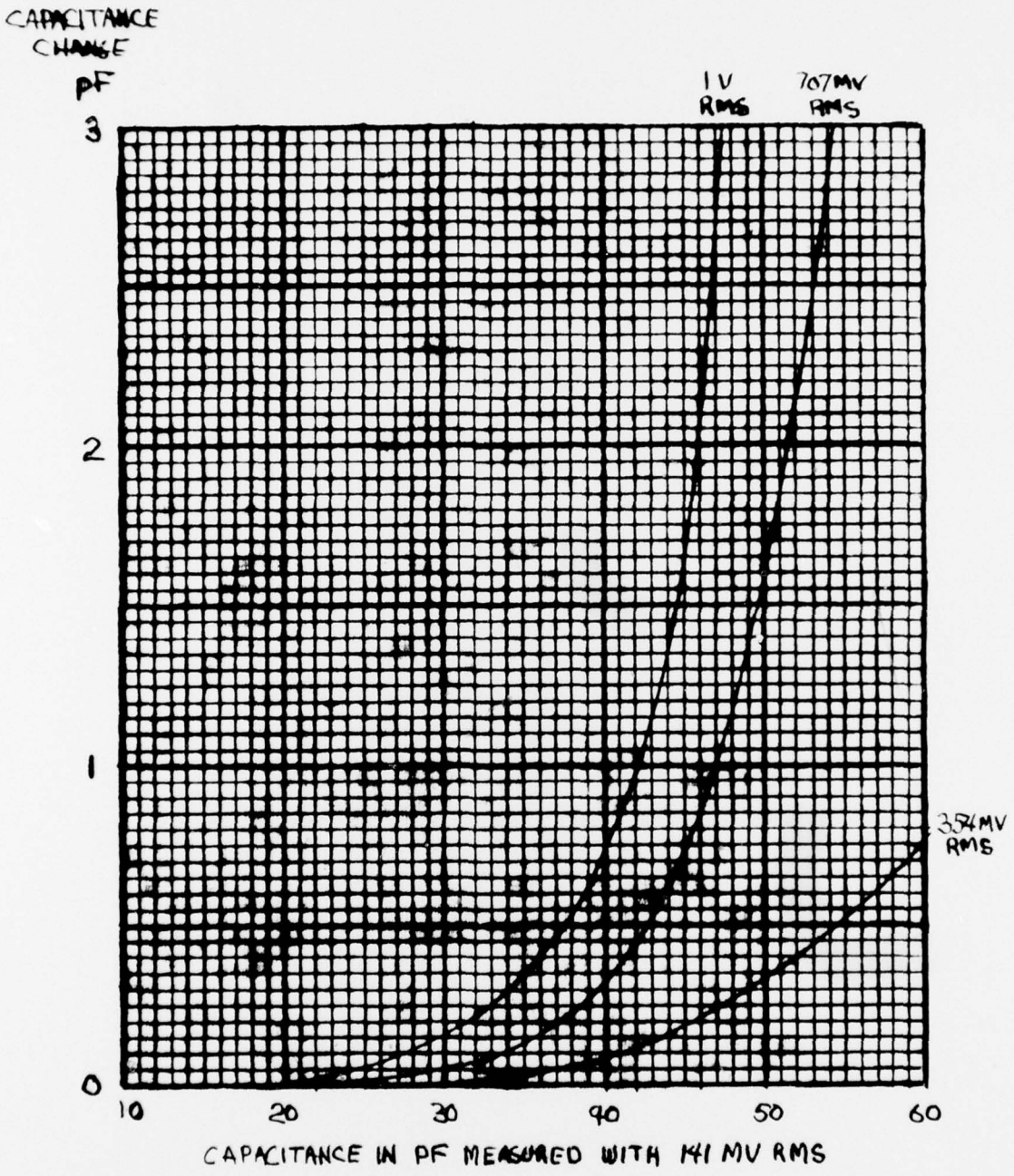


"RELCOM" BTBC 200/50Ω TRANSFORMERS



BRIDGE OUTPUT COUPLING AT 2 OHM BALANCE

FIGURE 8.4.3



VARACTOR CAPACITANCE CHANGE WITH RF VOLTAGE

FIGURE 8.6.1

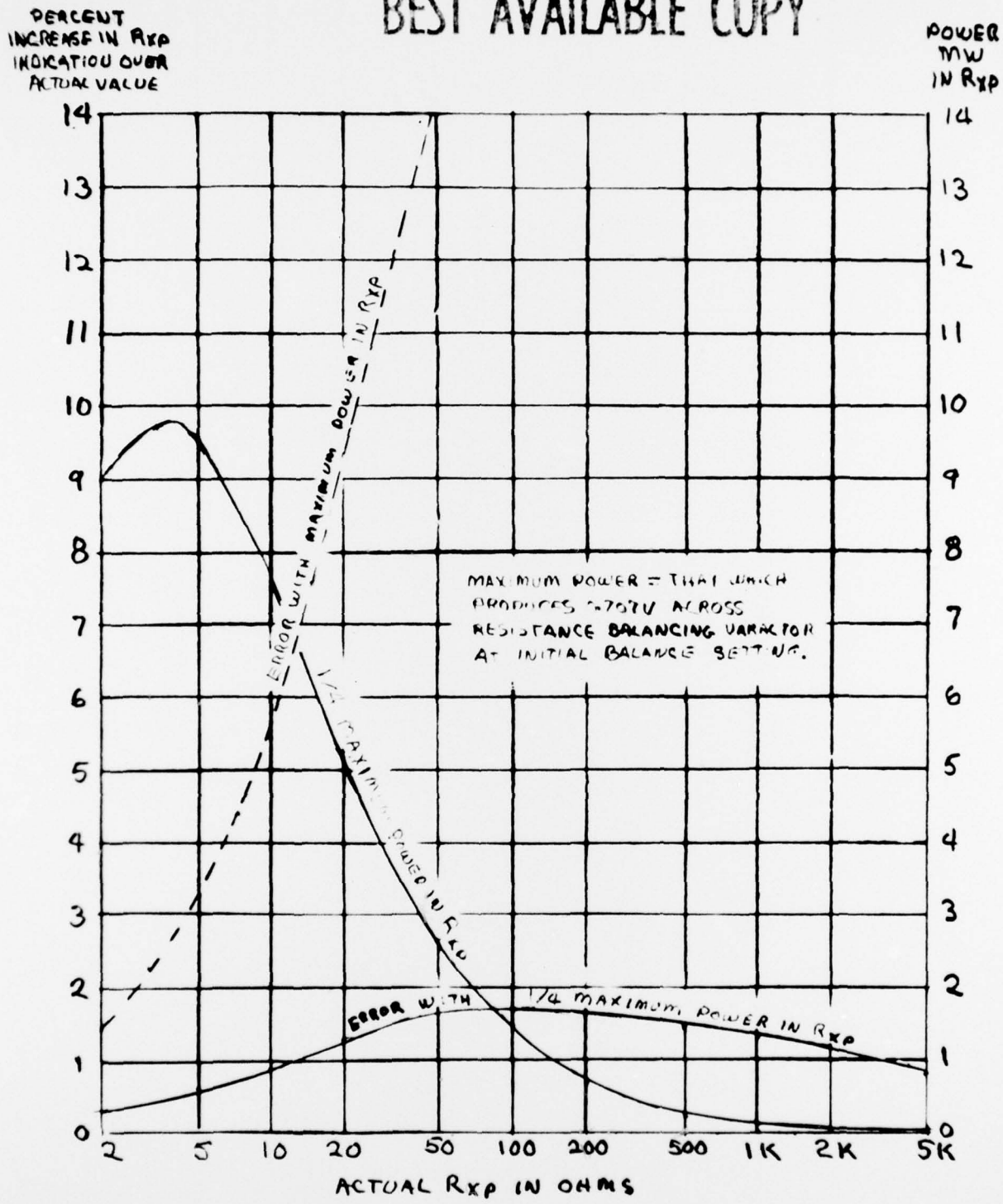


FIG. 8.6.2 RESISTANCE MEASURING ERROR AT HIGH RF DRIVE LEVELS

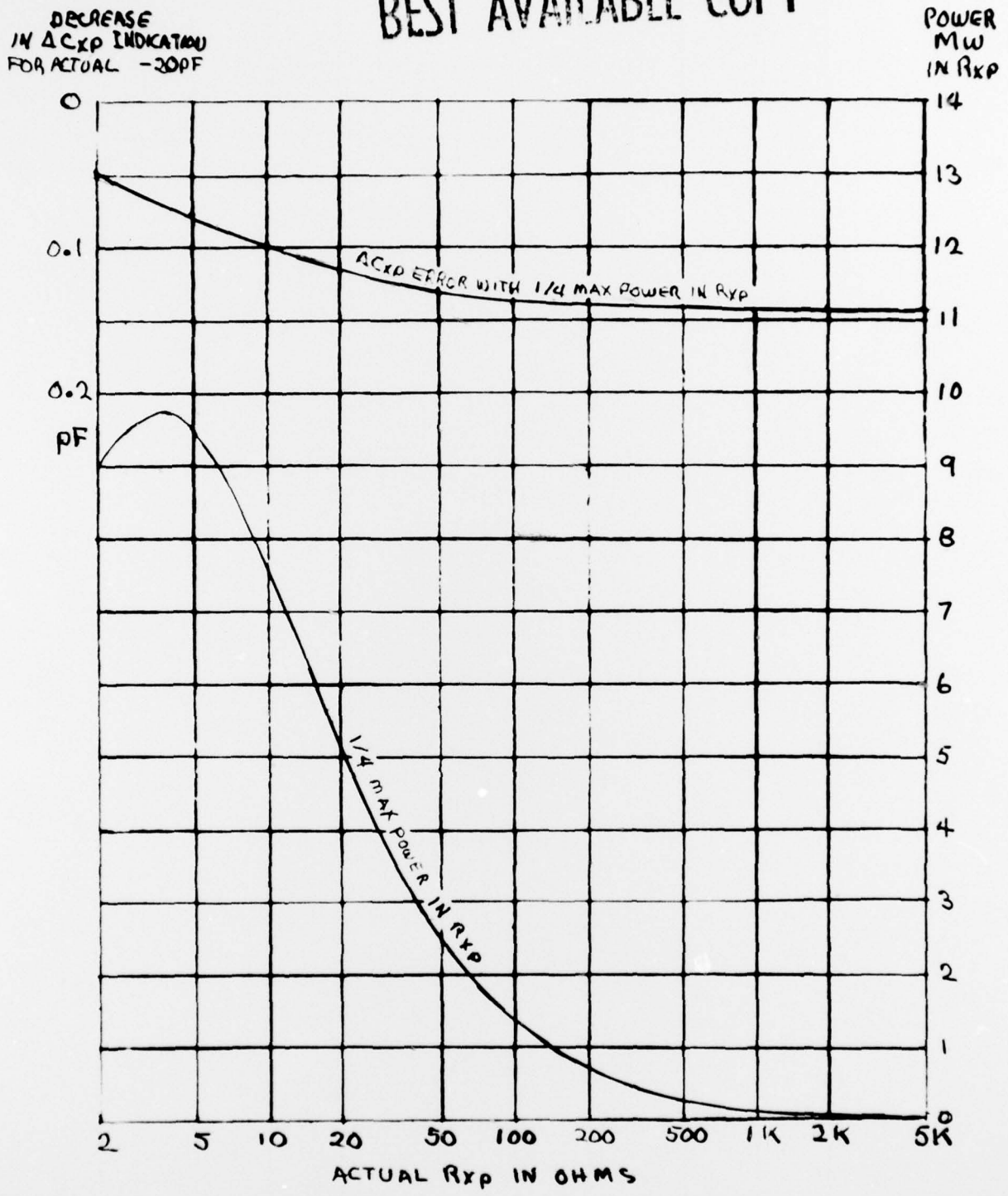


FIG. 8.6.3 CAPACITANCE MEASURING ERROR AT HIGH RF DRIVE LEVELS

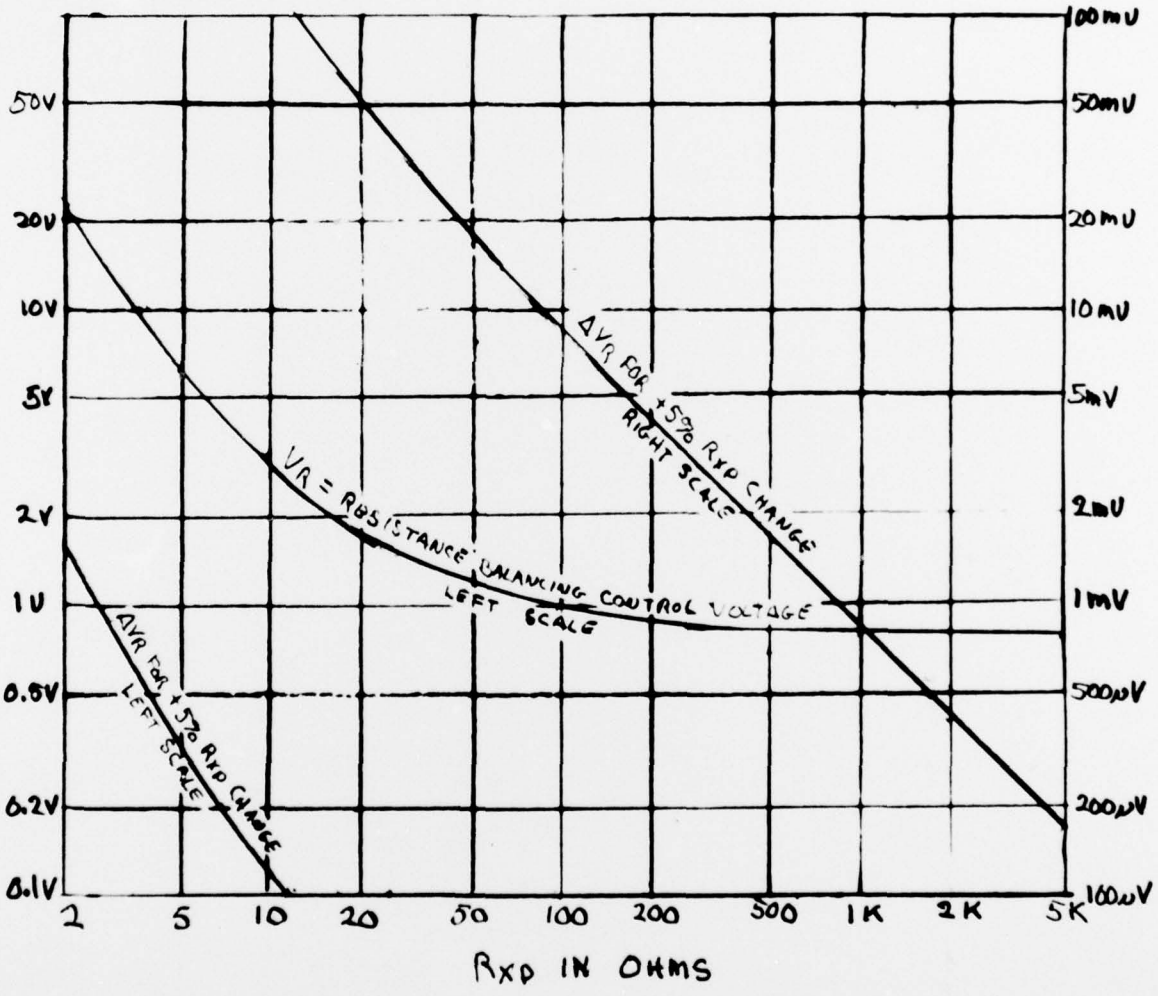
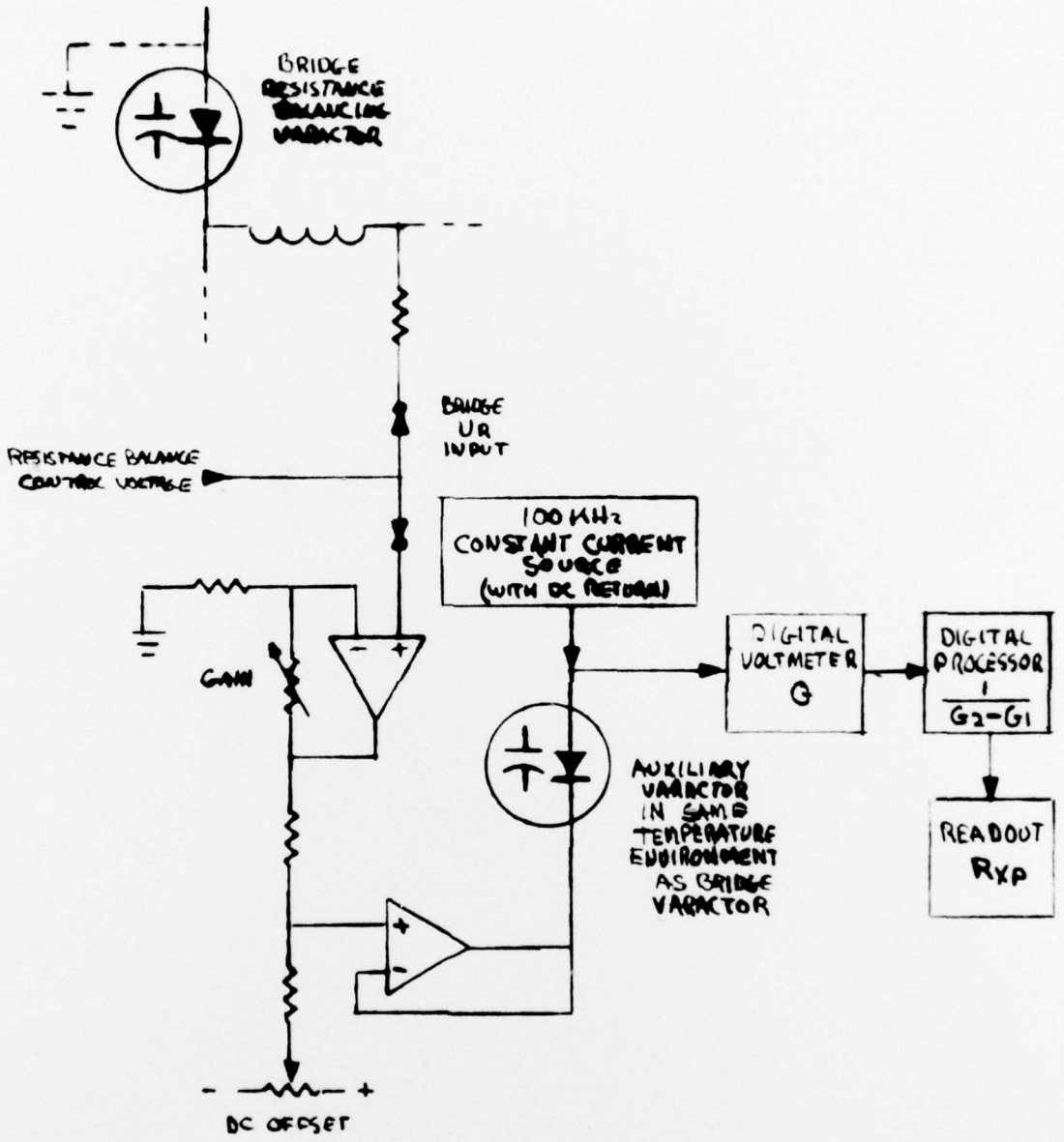


FIG. 9.2.1 RESISTANCE BALANCING CONTROL VOLTAGE AND READOUT RESOLUTION REQUIRED FOR A PLUS 5 PERCENT RESISTANCE CHANGE



POSSIBLE TEMPERATURE COMPENSATED CONVERTOR FOR RESISTANCE READOUT

FIGURE 9.2.2

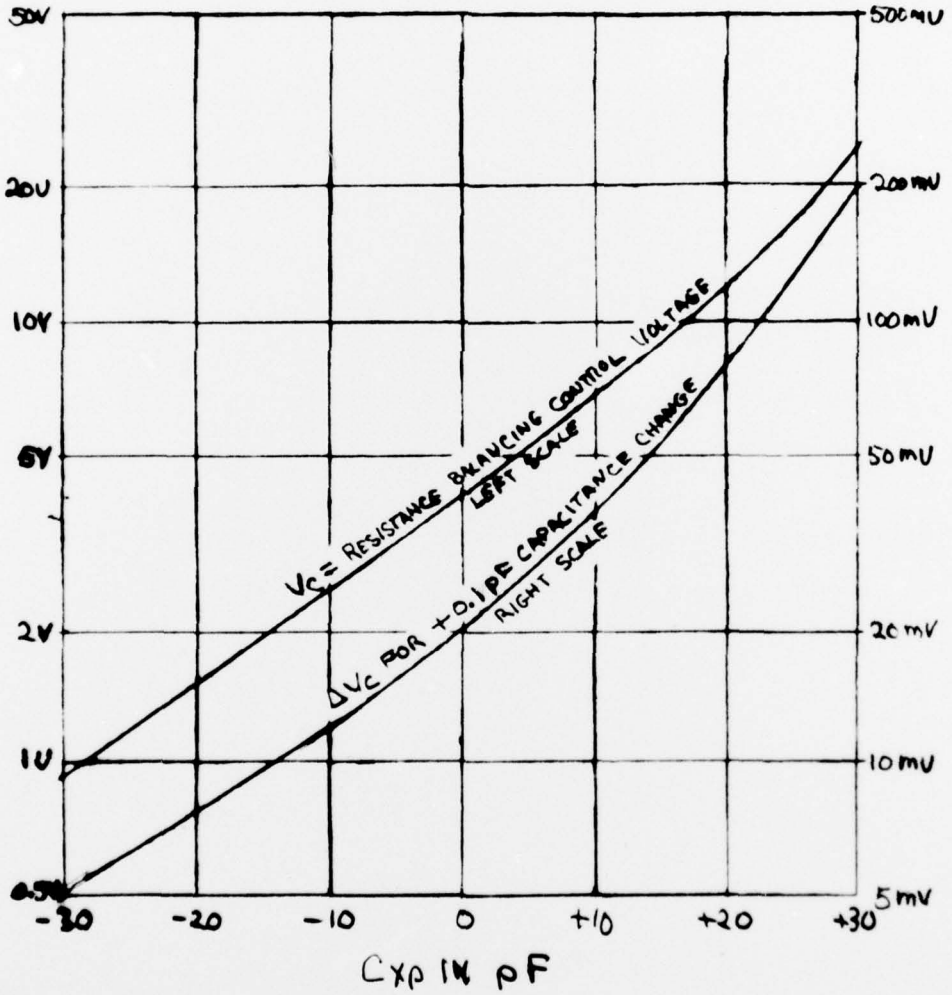
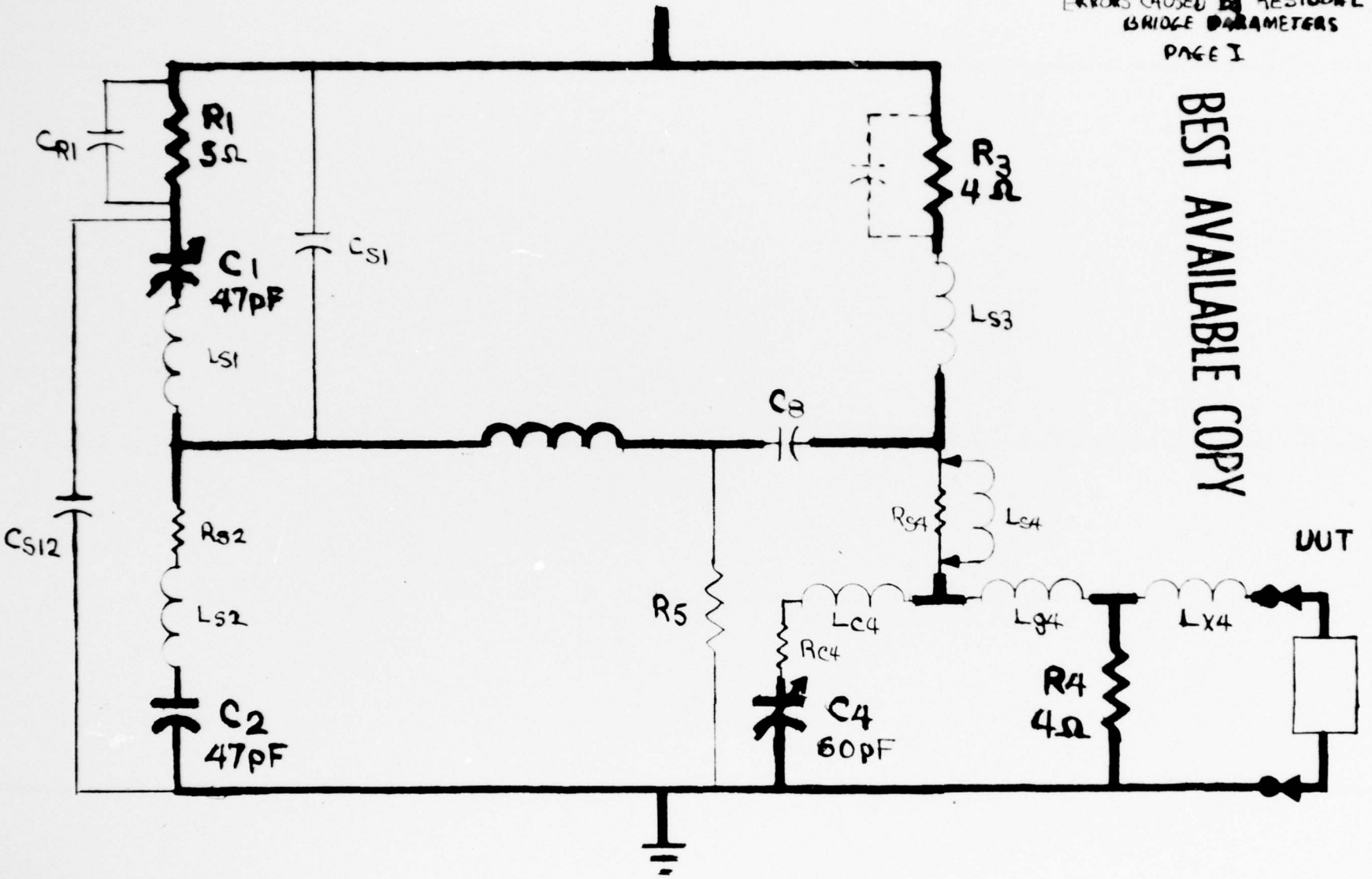
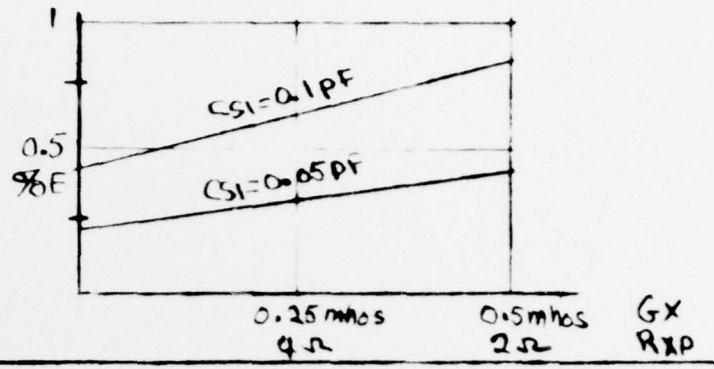
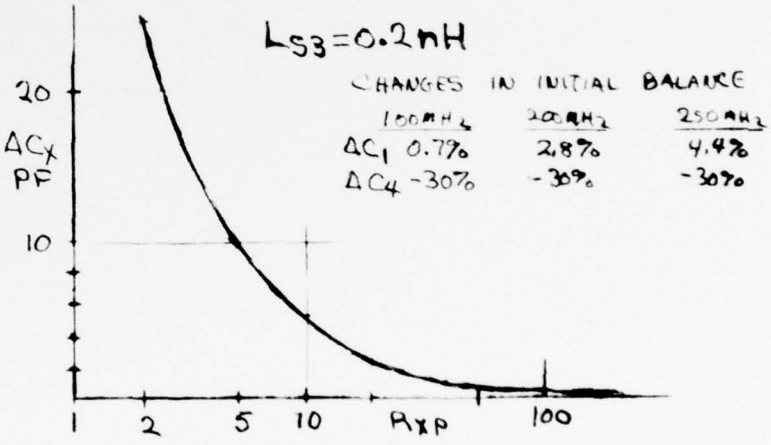
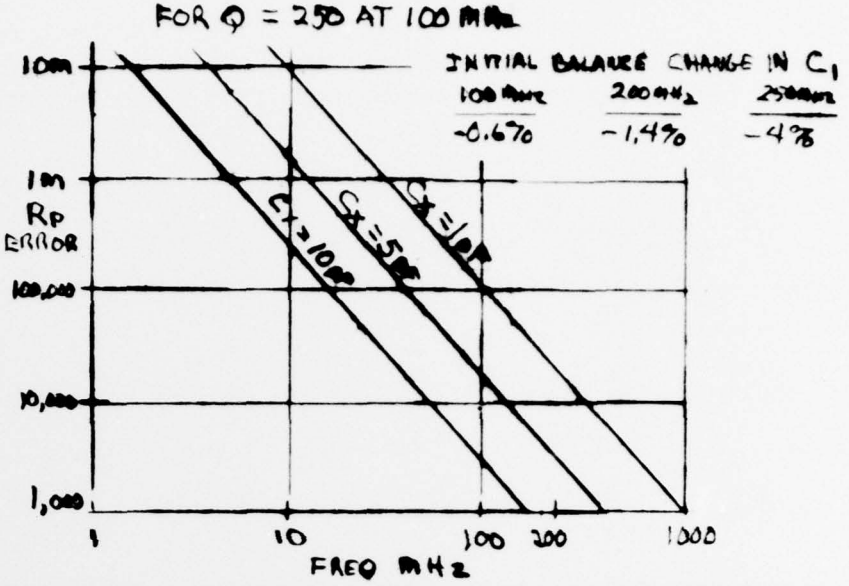
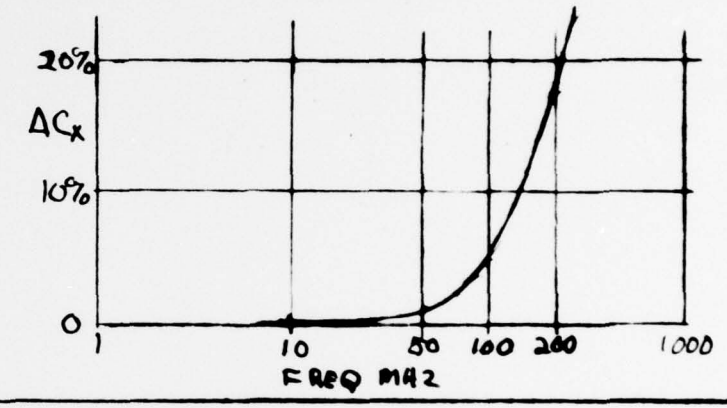


FIG. 9.3.1. CAPACITANCE BALANCING CONTROL VOLTAGE AND READOUT RESOLUTION REQUIRED FOR A PLUS 0.1 PF CAPACITANCE CHANGE

RESIDUAL BRIDGE PARAMETERS



ARM	RESIDUAL	ERROR	RESIDUAL RANGE	PLOT
1	C_{S1}	IN G_m= $\Delta G_m = -.85\, C_{S1}\,(G_x + 0.5)\%$ C_{S1} IN pF INDEPENDENT OF FREQ. IN C_m= SMALL, $< C_{S1}$	0 → 0.1pF	
	C_{S12}	$\Delta C_4 = \frac{R_1}{R_m} C_{S12}$ NEGLIGIBLE, ALWAYS SMALLER THAN C_{S12} $\Delta G_m \cong 0$		
	L_{S1}	INITIAL BALANCE SHIFT IN C_1 ONLY $\Delta C_1 = -\omega^2 L_{S1} C_1$	0 → 0.5nH	INITIAL BALANCE SHIFT IN C_1 WITH L_{S1} = 0.5 nH: 100 MHz −1%; 200 MHz −4%; 250 MHz −6.3%
3	L_{S3}	ERROR IN C_X $\Delta C_X = G_X \frac{L_{S3}}{R_3} = \frac{1}{R_{XP}} \frac{L_{S3}}{R_3} \times 10^{12}$ pF CHANGE IN INITIAL BALANCE $\Delta C_1 = \frac{\omega^2 L_{S3} C_4 R_4}{R_3}$ $\Delta C_4 = -\frac{L_{S3}}{C_4 R_3 R_4}$	0 → 0.2nH	

ARM	RESIDUAL	ERROR	RESIDUAL RANGE	PLOT
4	R_{C4} (Q of CAPACITANCE VARACTOR)	$G_{ERROR} = \frac{2\omega C_x}{Q_{C4}}$ mhos $= \frac{2\omega^2 C_{C4} C_x}{G_{C4}}$ mhos CHANGE IN C_1 INITIAL BALANCE $\Delta C_1 \cong -(\omega C_4)^2 R_4 R_{C4}$	Q = 250 AT 100 MHz INV ∝ FREQ G_{C4} = 4 mhos	
	L_{C4}	$\Delta C_x = \frac{C_x \text{ ERROR}}{200\omega^2 L_{C4} C_{41}}$ %	L_{C4} = 2nH (C_{41} = 60pF)	
	L_{X4}	$\frac{1}{R_m} = \frac{\frac{1}{R_x}}{(1-\omega^2 L_{X4} C_x)^2 + \left(\frac{\omega L_{X4}}{R_x}\right)^2}$ $C_m = \frac{C_x - \frac{L_{X4}}{R_x^2} - \omega^2 L_{X4} C_x}{(1-\omega^2 L_{X4} C_x)^2 + \left(\frac{\omega L_{X4}}{R_x}\right)^2}$	0 → 0.5 nH	THIS IS AN IMPORTANT CROSS ERROR, PARTICULARLY WHEN LOW VALUED RESISTANCES ARE MEASURED.